

AC6969E Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: V1.6

Date: 2026.08.04

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

AC6969E Features

CPU

- 32-bit DSP supports hardware Float Point Unit (FPU)
- Up to 160MHz programmable processor
- 64 Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codecs supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC, AES)
- Single MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 10-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC, SNR $\geq$ 95dB
- One channels 16-bit ADC, SNR $\geq$ 90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Two channels Mono analog MUX
- Supports single-ended DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V6.0+BR+EDR+BLE specification (DN Q382031)
- Meet class2 and class3 transmitting power requirement

- Support GFSK and $\pi/4$ DQPSK all packet types
- Provides maximum +6dbm transmitting power
- Receiver with minimum -90dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile
- a2dp 1.4\avctp 1.4\avdtp 1.3\ avrcp 1.6.3\ hfp 1.9\spp 1.2\rfcomm 1.2\pnp 1.3\ hid 1.1.1\sdp core 6.0\l2cap core 6.0

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, UART0 and UART1 supports DMA mode
- One hardware IIC interface supports host and device mode
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

PMU

- Low voltage LDO for internal digital and analog circuit supply
- 3uA current consumption in the soft-off mode
- Built-in LDO for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 5V
- VDDIO is 2.2V to 3.6V

Packages

- SOP16

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

 Bluetooth speaker

ZHUHAI JIELI TECHNOLOGY CO., LTD

1、 Pin Definition

1.1 Pin Assignment

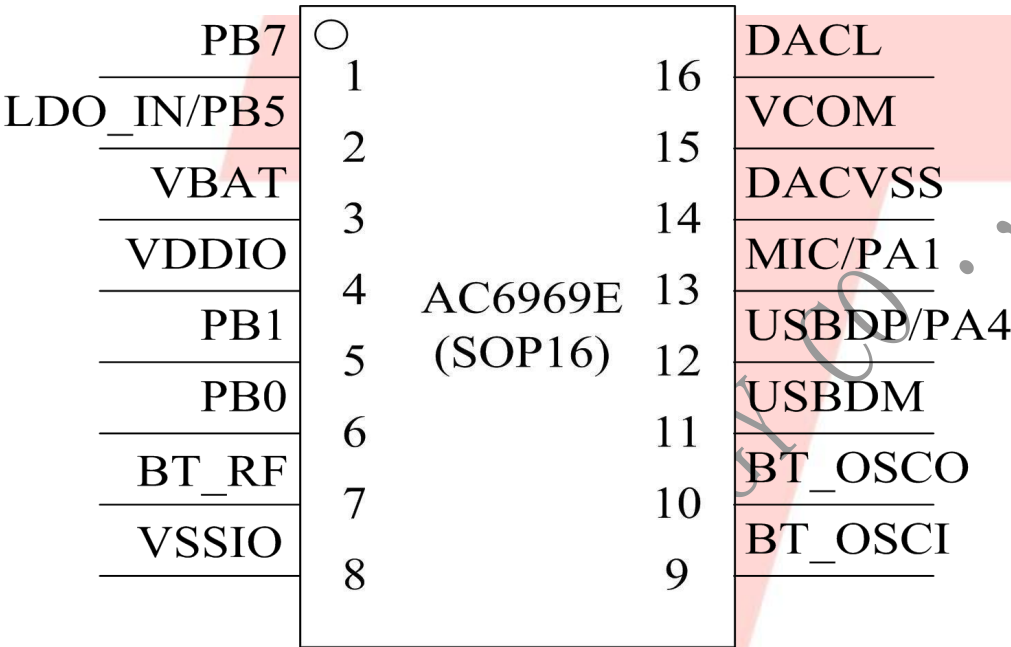


Figure 1-1 AC6969E Package Diagram

1.2 Pin Description

Table 1-1 AC6969E Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	DACR	O	/		DAC Right Channel
	PB7	I/O	24/8	GPIO	SD0CLK_BF: SD0Clock(BF) AMUX1R: Analog Channel1Right; SPI2DOA: SPI2 Data Out(A); IIC_SDA_C: IIC DAT(C); ADC9: ADC Input Channel 9; PWM5: Timer5 PWM Output; UART1RXA: Uart1 Data In(A);
2	LDO_IN	P	/		Battery Charger In
	PB5	I/O	8	GPIO (High Voltage Resistance)	SPI2DIA: SPI2 Data Input(A); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture; UART0TXC: Uart0 Data Out(C); UART0RXC: Uart0 Data In(C);
3	VBAT	P	/		Battery Power Supply
4	VDDIO	P	/		IO Power 3.3v
5	PB1	I/O	24/8	GPIO (pull up)	Long Press Reset; SPI1DOA: SPI1 Data Out(A); ADC5: ADC Input Channel 5; TMR2: Timer2 Clock Input; UART0RXB: Uart0 Data In(B); SPDIF_IN_D: Sony/Philips Digital Interface Input(D)
6	PB0	I/O	8	GPIO (High Voltage Resistance)	SD0CLK_D: SD0Clock(D) SPI1CLKA: SPI1 Clock(A); UART0TXB: Uart1 Data Out(B); TMR5: Timer5 Clock Input; SPDIF_IN_C: Sony/Philips Digital Interface Input(C)
7	BT_RF	/	/		BT Antenna
8	VSSIO	P	/		Ground
9	BT_SOCI	I	/		BT OSC In
10	BT_SOCO	O	/		BT OSC Out
11	USBDM	I/O	4	USB Negative	SPI2DOB: SPI2 Data Out(B);

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

				Data (pull down)	IIC_SDA_A: IIC SDA(A); ADC14: ADC Input Channel 14; UART1RXD: Uart1 Data In(D);
12	USBDP	I/O	4	USB Positive Data (pull down)	SPI2CLKB: SPI2 Clock(B); IIC_SCL_A: IIC SCL(A); ADC13: ADC Input Channel 13; UART1TXD: Uart1 Data Output(D);
	PA4	I/O	24/8	GPIO	SD0CMDC: SD0 Command(C) AMUX0R: Analog Channel0 Right; UART1_RTS: Uart1 Request to send; ADC3: ADC Input Channel 3; TMR4: Timer4 Clock Input; UART2RXA: Uart2 Data In(A);
13	PA1	I/O	24/8	GPIO	MIC: MIC Input Channel; ADC1: ADC Input Channel 1; PWM4: Timer4 PWM Output; UART1RXC: Uart0 Data In(C);
14	DACVSS	P	/		DAC Ground
15	VCOM	/	/		
16	DACL	O	/		DAC Left Channel

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-20	+70	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	2.2	5.5	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	VDDIO+0.3	V
LDO_IN	Charge Input Voltage	-0.3	6	V

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Loading current	—	—	300	mA	VBAT = 4.2V
VBAT	Voltage Input	2.2	3.7	5	V	
V _{DVDD}	Voltage output	0.9	1.2	1.25	V	VBAT = 4.2V, 30mA loading
V _{VDDIO}	Voltage output	—	3.3	—	V	VBAT = 4.2V, 100mA loading
V _{BT_AVDD}	Voltage output	—	1.3	—	V	VBAT=4.2V, 100mA loading

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	—
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	—
I _{Charge}	Charge Current	20		300	mA	Charge current at fast charge mode
I _{Trinkl}	Trickle Charge Current	20	45	70	mA	V _{BAT} <V _{Trinkl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	—	$0.3 \times V_{DDIO}$	V	$V_{DDIO} = 3.3V$
V_{IH}	High-Level Input Voltage	$0.7 \times V_{DDIO}$	—	$V_{DDIO} + 0.3$	V	$V_{DDIO} = 3.3V$
IO output characteristics						
V_{OL}	Low-Level Output Voltage	—	—	0.33	V	$V_{DDIO} = 3.3V$
V_{OH}	High-Level Output Voltage	2.7	—	—	V	$V_{DDIO} = 3.3V$

2.5 Internal Resistor Characteristics

Table 2-5

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1,PA4 PB1,PB7	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance accuracy $\pm 20\%$
PB0,PB5	8mA	—	10K	10K	
USBDP	4mA	—	1.5K	15K	
USBDM	4mA	—	180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	—	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	—	-75	—	dB	
S/N	—	95	—	dB	
Crosstalk	—	-90	—	dB	
Output Swing	—	1	—	Vrms	1KHz/-60dB 10Kohm loading With A-Weighted Filter
Dynamic Range	—	95	—	dB	
DAC Output Power	—	20	—	mW	

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		80		dB	1KHz/-60dB
S/N	—	90	91	dB	1KHz/-60dB
THD+N	—	-70	—	dB	
Crosstalk	—	-90	—	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		4	6	dBm	25°C, Power Supply VBAT=4.2V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate

Table 2-9

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-1		dB	25°C, Power Supply VBAT=4.2V 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS	6		%	
	DEVM 99%	10		%	
	DEVM Peak	15		%	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.8.2 Receiver

Basic Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=4.2V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
Interference Rejection	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate

Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=4.2V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
Interference Rejection	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 SOP16

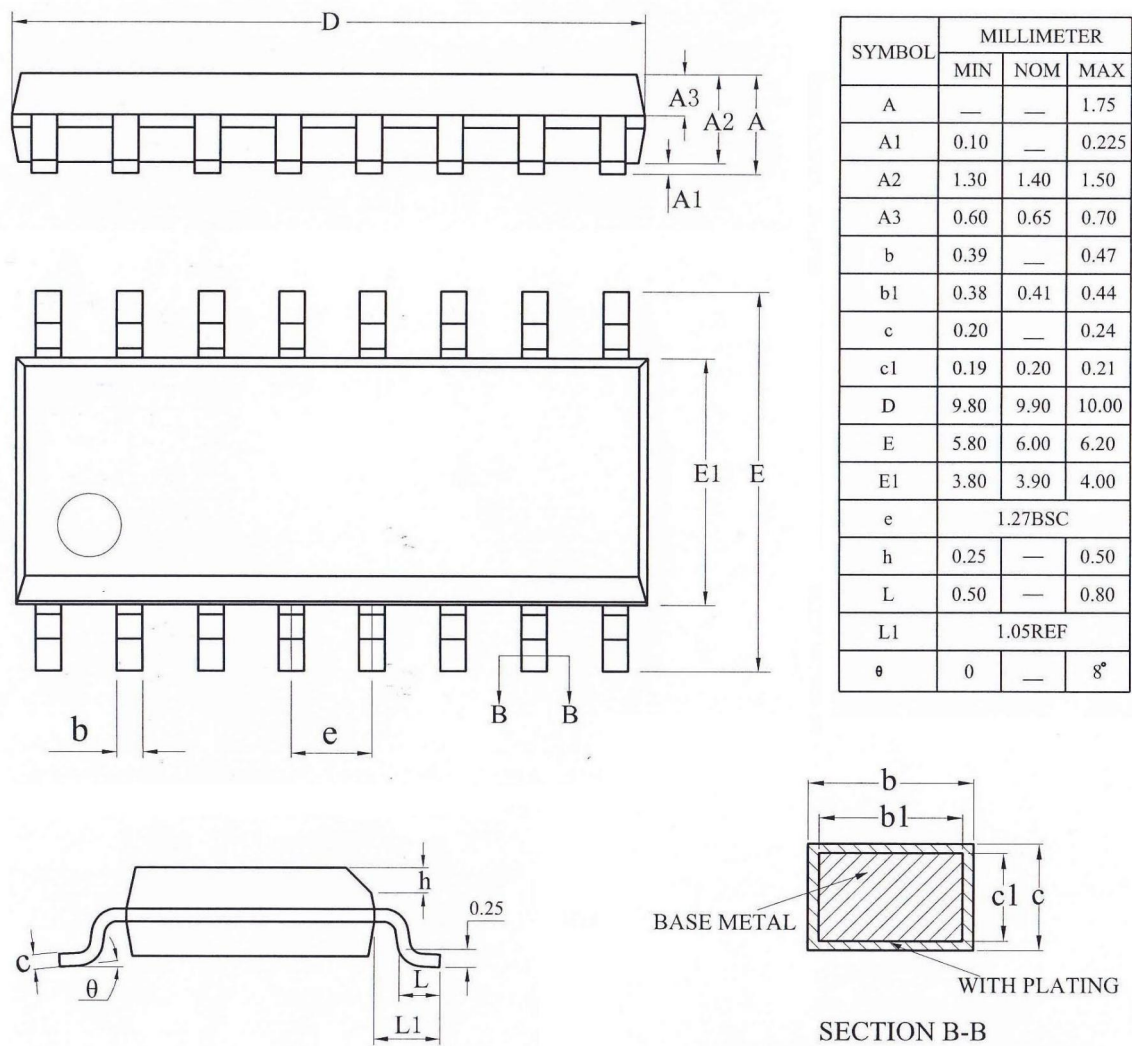


Figure 3-1. AC6969E_SOP16 Package

3、Revision History

Date	Revision	Description
2020.06.02	V1.0	Initial Release
2021.11.22	V1.1	Update Bluetooth Vision and profiles, Update Audio characters
2024.10.08	V1.2	Update Bluetooth Vision and profiles
2025.01.09	V1.3	Update Bluetooth Vision and profiles
2026.03.21	V1.4	Update PMU Characteristics
2026.04.03	V1.5	Update Pin Description and PMU Characteristics
2026.08.04	V1.6	Update Bluetooth DN and PMU Characteristics

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.