JL7106F Datasheet

Zhuhai Jieli Technology Co.,LTD

Version V1.4

Date 2025.08.29

Revision History

Date	Revision	Description
2025.01.15	V1.0	Initial Release
2025.03.14	V1.1	Update IC Marking Information
2025.04.16	V1.2	Update Datasheet Format Update Package Information
2025.06.13	V1.3	Update Features_SYSTEM Update Features_Audio Update Audio DAC Characteristics
2025.08.29	V1.4	Update Features_Audio Update Pin Description(the differences in I/O Functions among different versions of chips)

Table of Contents

JL7106F Features

SYSTEM

- 32bit Single-core DSP 192MHz
- On-chip SRAM 240kbyte
- With IEEE754 Single precision FPU
- Support FFT/MATRIX/MATH
- I-cache and D-cache
- Support EMU
- Support MMU
- Support MPU
- Built-In Flash
- 24MHz crystal oscillator
- Internal RC oscillator,PLL

DSP Audio Processing

- SBC/AAC/LDAC/LHDC/LC3/CVSD/mSBC codec
- mSBC voice codec supported for BT phone
- PLC for voice processing
- Single/Dual MIC ENC
- Multi-band DRC
- Multi-band EQ
- Support spatial sound
- Support assistive listening
- Support Hi-Res Audio

ANC

- Wide band digital adaptive ANC
- Support hybrid/feedforward/feedback
- Support wind noise detection
- Support wide area tap
- Support Speak-to-Chat
- Support tip fit test & wear detection
- Input-to-output latency
  - 10us@SR=750kHz
  - 14us@SR=375kHz

Audio

- 2 x 24bit DAC
  - SNR 119dB
  - Noise 1uVrms
  - Support differential mode
  - Support VCMO mode
  - Sampling rate 8~384kHz
- 2 x 24bit ADC
  - SNR 100dB
  - Sampling rate 8~192kHz
  - Support analog/digital microphone
- 1 x I^2S AUDIO Master/Slave interface
  - Sampling rate 8~384kHz
  - Support TX and RX
  - Support multi-slot mode(TDM)

Bluetooth

- Dual-mode BT6.0 with LE Audio (DN Q332415)
- Support AoA
- Support LE audio BIS/CIS
- Maximum transmitting power 13dBm
- Receiver sensitivity
  - -94dBm @BR
  - -95dBm @EDR Π/4 DQPSK
  - -87dBm @EDR 8DPSK

Peripherals

- 1 x Full speed USB
- 1 x SD host controller
- 4 x Multi-function 32bit timer
- 2 x UART interface
- 1 x I^2C Master/Slave interface
- 2 x SPI Master/Slave interface
- 1 x QDEC
- 1 x 10bit ADC(12 Channels)
- 4 x MCPWM
- 2 x LP_Touch with low power wake up
- 4 x IR RX
- 15 x GPIO Support function remapping

PMU

- Integrated battery charger up to 225mA
- 1 x Buck DC-DC converter
- Support temperature sensor
- VPWR range 4.5V to 5.5V
- VBAT range 2.7V to 4.5V

- IOVDD range 2.7V to 3.6V
- TWS Power < 4.4mA
  @AAC No-Load VBAT=3.7V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature
  TC = -20℃ to +85℃(standard range)
  TC = -40℃ to +105℃(extended range)
- Storage temperature -65℃ to +150℃

Applications

- ANC TWS/OWS
- Adaptive ANC headphone
- Bluetooth audio device

1 Block Diagram

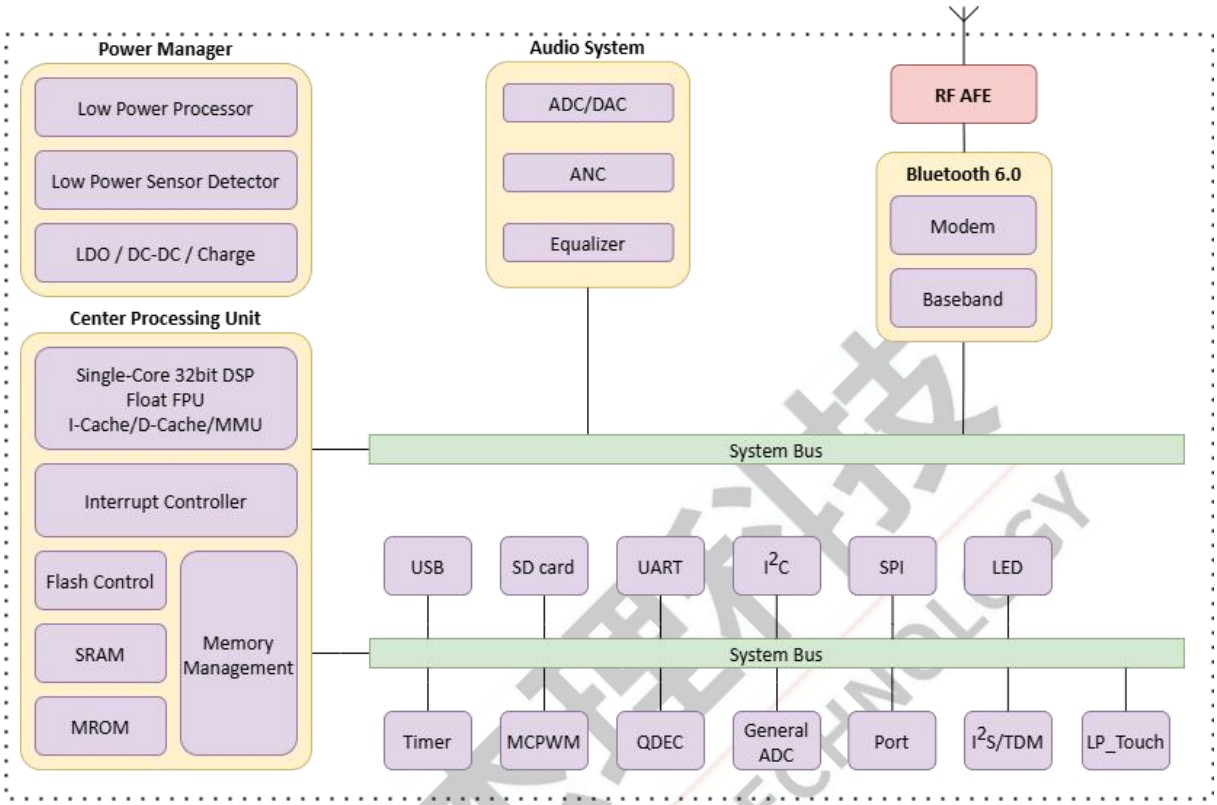


Figure 1-1 JL7106F Block Diagram

2 Pin Definition

2.1 Pin Assignment

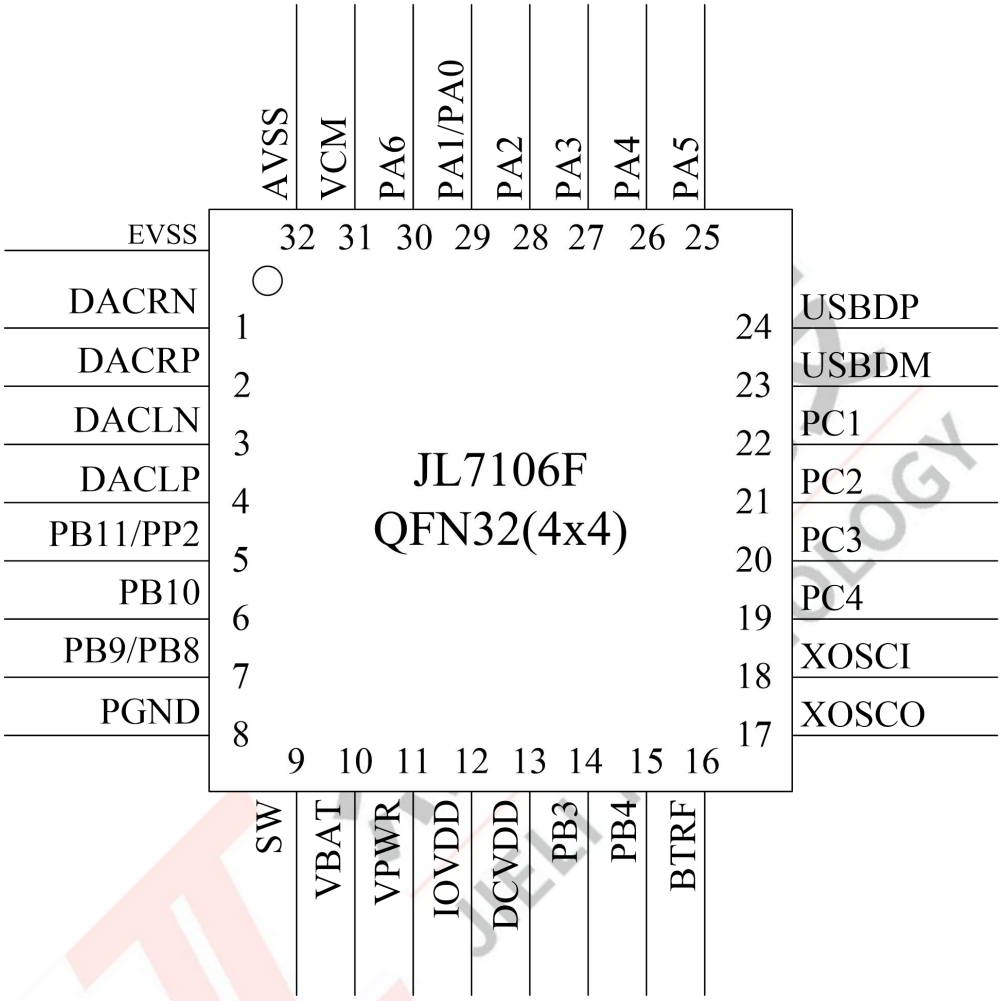


Figure 2-1 JL7106F Pin Assignment

2.2 Pin Description

Table 2-2-1 JL7106F Pin Description

Pin No.	Name	Type	IO Initial State	Description
1	DACRN	P	--	Right Channel DAC Negative Output
2	DACRP	P	--	Right Channel DAC Positive Output
3	DACLN	P	--	Left Channel DAC Negative Output DAC VCMO Output
4	DACLP	P	--	Left Channel DAC Positive Output
5	PB11	I/O	Z	MICBIASB(MIC Bias Output) MIC_B0(MIC Input)
	PP2	I/O	Z	SDPG(SD Power) ADC13(ADC Input Channel 13)
6	PB10	I/O	Z	AIN_B0(Audio ADC Positive Input)
7	PB9*	I/O	Z	**Chip Version A/B/C :** AIN_B1(Audio ADC Positive Input) AIN_BN(Audio ADC Negative Input)
				Chip Version D : AIN_BN(Audio ADC Negative Input)
	PB8*	I/O	Z	**Chip Version A/B/C :** ADC12(ADC Input Channel 12)
				Chip Version D : AIN_B1(Audio ADC Positive Input) ADC12(ADC Input Channel 12)
8	PGND	G	--	Ground of Buck DC-DC converter
9	SW	P	--	Buck DCDC Switch Port
10	VBAT	P	--	Battery Input
11	VPWR	P	--	Charge Power Input
12	IOVDD	P	--	IO Power
13	DCVDD	P	--	1.25V DCDC Power
14	PB3	I/O	Z	LP_TOUCH4(TOUCH_CH4) ADC10(ADC Input Channel 10)
15	PB4	I/O	10kΩ Pull-up	Hold down 0 to reset LP_TOUCH5(TOUCH_CH5) ADCP0(ADC Input Channel P0)
16	BTRF	RF	--	Bluetooth RF Antenna
17	XOSCO	O	--	Crystal Oscillator Output
18	XOSCI	I	--	Crystal Oscillator Input
19	PC4	I/O	Z	ADC3(ADC Input Channel 3)
20	PC3	I/O	Z	ADC2(ADC Input Channel 2)
21	PC2	I/O	Z	ADC1(ADC Input Channel 1)

Pin No.	Name	Type	IO Initial State	Description
22	PC1	I/O	Z	ADC0(ADC Input Channel 0)
23	USBDM	I/O	15kΩ Pull-down	USB Negative Data ADC15(ADC Input Channel 15)
24	USBDP	I/O	15kΩ Pull-down	USB Positive Data ADC14(ADC Input Channel 14)
25	PA5	I/O	Z	ADC6(ADC Input Channel 6)
26	PA4	I/O	Z	ADC5(ADC Input Channel 5)
27	PA3*	I/O	Z	**Chip Version A/B/C :** ADC4(ADC Input Channel 4)
				Chip Version D : ADC4(ADC Input Channel 4) AIN_A1(Audio ADC Positive Input)
28	PA2*	I/O	Z	**Chip Version A/B/C :** AIN_A1(Audio ADC Positive Input) AIN_AN(Audio ADC Negative Input)
				Chip Version D : AIN_AN(Audio ADC Negative Input)
29	PA1	I/O	Z	AIN_A0(Audio ADC Positive Input)
	PA0	I/O	Z	MICBIASA(MIC Bias Output) MIC_A0(MIC Input)
30	PA6	I/O	Z	--
31	VCM	P	--	Audio reference voltage
32	AVSS	G	--	Audio Ground

Note

1.IO initial state abbreviations Z--High resistance, H--High level, L--Low level, X--May be changed during power on.

2.Timer, MCPWM, QDEC, UART, LEDC, I^2C, I^2S, SPI,IR RX and SD functions can be remapped to any I/O.

3.* indicates that this pin function is related to the chip version.

Table 2-2-2 Pin Types Description

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
G	Ground	I	Input
RF	RF antenna	O	Output

2.3 Pin Specialist

Table 2-3 Pin keep Description

Pin	Description for IOVDD power off mode
PC1	Support driving and sampling external 100kΩ NTC resistance in single IO
PB4	10kΩ Pull-up and Hold down 0 to reset function can be disable by efuse in IO Initial State

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-20	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	4.5	V
VPWR		-0.3	6	V
IOVDD		-0.3	3.6	V
DCVDD		-0.3	1.55	V
GPIO	Input voltage of GPIO	-0.3	3.6	V

Note

1.Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

3.2 ESD Ratings

Table 3-2 ESD Ratings

Parameter	Typ	Test pin	Reference standard
Human Body Mode	±4kV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±300V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2kV	All pins	ANSI/ESDA/JEDEC JS-002-2022

3.3 PMU Characteristics

Table 3-3 PMU Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Power supply	--	2.7	3.7	4.5	V
VPWR	Power supply	--	4.5	5.0	5.5	V
Operating mode						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
IOVDD	Voltage output	--	--	3	--	V
	Loading current	IOVDD=3.0V@VBAT = 3.7V or VPWR=5V	--	--	120	mA
DCVDD	Voltage output	--	--	1.25	--	V
	Loading current	DCVDD=1.25V@IOVDD=3.0V in LDO mode	--	--	120	mA
		DCVDD=1.25V@VBAT=3.7V in DCDC mode	--	--	120	mA
Low Power mode						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
IOVDD	Loading current	IOVDD=3.0V@VBAT = 3.7V or VPWR=5V	--	--	10	mA

3.4 Battery Charge

Table 3-4 Charger Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VPWR	Charge Input Voltage	4.5	5	5.5	V
CV	CV Mode Voltage Accuracy	4.175	4.2	4.225	V
		4.375	4.4	4.425	V
		4.475	4.5	4.525	V
CC	CC Mode Current	30	--	225	mA
I_{end}	End Of Charge Current	3	--	22.5	mA
V_{Trikl}	Trickle Charge Voltage	--	3	--	V

3.5 IO Characteristics

Table 3-5 IO Characteristics

Input Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Min**	**Max**	**Unit**
V_{IL}	Low-Level Input Voltage	IOVDD = 3.0V	PA0~PA6 PB3,PB4,PB8~PB11 PC1~PC4 PP2 VPWR USBDP USBDM	-0.3	1.3	V
V_{IH}	High-Level Input Voltage	IOVDD = 3.0V	PA0~PA6 PB3,PB4,PB8~PB11 PC1~PC4 PP2 USBDP USBDM	1.7	3.3	V
		IOVDD = 3.0V	VPWR	1.7	5.5	V
Output Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Typ**		**Unit**
| I_{OL} |	Output Current	IOVDD = 3.0V Voutput = 0.3V	PA0~PA6 PB3,PB4,PB8~PB11 PC1~PC4	1(HD=0) 4(HD=1) 8(HD=2) 31(HD=3)		mA
		IOVDD = 3.0V Voutput = 0.3V	USBDP USBDM	8		mA
		IOPP2VDD = 3.0V Voutput = 0.3V	PP2	30(HD=0) 300(HD=1)		mA
		IOVDD = 3.0V	VPWR	2		mA

		Voutput = 0.3V			
| I_{OH} |	Output Current	IOVDD = 3.0V Voutput = 2.7V	PA0~PA6 PB3,PB4,PB8~PB11 PC1~PC4	1(HD=0) 4(HD=1) 8(HD=2) 31(HD=3)	mA
		IOVDD = 3.0V Voutput = 2.7V	USBDP USBDM	8	mA
		IOVDD = 3.0V Voutput = 2.7V	PP2	30(HD=0) 300(HD=1)	mA
		IOVDD = 3.0V Voutput = 2.7V	VPWR	2	mA
Internal Resistance Characteristics					
Symbol	**Parameter**	**Conditions**	**IO**	**Typ**	**Unit**
R_{pu}	Pull-up Resistance	IOVDD = 3.0V	PA0~PA6 PB3,PB4,PB8~PB11 PC1~PC4 PP2 VPWR	10k(PU=1) 200k(PU=2) 1M(PU=3)	Ω
		IOVDD = 3.0V	USBDP	1.5k 10k(PU=1) 200k(PU=2) 1M(PU=3)	Ω
		IOVDD = 3.0V	USBDM	180k 10k(PU=1) 200k(PU=2) 1M(PU=3)	Ω
R_{pd}	Pull-down Resistance	IOVDD = 3.0V	PA0~PA6 PB3,PB4,PB8~PB11 PC1~PC4 PP2 VPWR	10k(PD=1) 200k(PD=2) 1M(PD=3)	Ω
		IOVDD = 3.0V	USBDP USBDM	15k 10k(PU=1) 200k(PU=2) 1M(PU=3)	Ω

Note

1. Internal pull-up/pull-down resistance accuracy ±20%

3.6 Audio DAC Characteristics

Table 3-6-1 Stereo DAC Characteristics (HPVDD Under 1.25V)

Parameter	Conditions		Min	Typ	Max	Unit
Resolution	--		--	24	--	bits
Input Sample Rate	--		8	--	384	kHz
SNR①	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	116	--	dB
	VCMO Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	110	--	dB
Dynamic Range	Differential Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	105	--	dB
	VCMO Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	97	--	dB
THD+N	Differential Mode Fin=1kHz@-0.5dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=32Ω	--	-80	--	dB
	VCMO Mode Fin=1kHz@-0.5dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=32Ω	--	-65	--	dB
Noise Floor	Differential Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	4.5	--	uVrms
	VCMO Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	4.5	--	uVrms
Noise Floor with MUTE	Differential Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	1	--	uVrms
	VCMO Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=16Ω	--	1	--	uVrms

Stereo Crosstalk	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=10kΩ	--	-120	--	dB
	VCMO Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.25V Load=10kΩ	--	-100	--	dB
Max Output Power	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted THD+N＜0.1%	HPVDD=1.25V Load=16Ω	--	30	--	mW
	VCMO Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted THD+N＜0.1%	HPVDD=1.25V Load=16Ω	--	7	--	mW

Table 3-6-2 Stereo DAC Characteristics (HPVDD Under 1.55V)

Parameter	Conditions		Min	Typ	Max	Unit
Resolution	--		--	24	--	bits
Input Sample Rate	--		8	--	384	kHz
SNR①	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	119	--	dB
	VCMO Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	113	--	dB
Dynamic Range	Differential Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	107	--	dB
	VCMO Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	99	--	dB
THD+N	Differential Mode Fin=1kHz@-0.5dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=32Ω	--	-80	--	dB

	VCMO Mode Fin=1kHz@-0.5dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=32Ω	--	-60	--	dB
Noise Floor	Differential Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	4.5	--	uVrms
	VCMO Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	4.5	--	uVrms
Noise Floor with MUTE	Differential Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	1	--	uVrms
	VCMO Mode Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=16Ω	--	1	--	uVrms
Stereo Crosstalk	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=10kΩ	--	-120	--	dB
	VCMO Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	HPVDD=1.55V Load=10kΩ	--	-100	--	dB
Max Output Power	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted THD+N＜0.1%	HPVDD=1.55V Load=16Ω	--	50	--	mW
	VCMO Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted THD+N＜0.1%	HPVDD=1.55V Load=16Ω	--	11.7	--	mW

Note

1. ①SNR is the ratio of output level with a 1kHz full-scale input to output level with MUTE on.

3.7 Audio ADC Characteristics

Table 3-7 Audio ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	24	--	bits
Output Sample Rate	--	8	--	192	kHz
SNR	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	100	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	98	--	dB
Dynamic Range	Differential input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	100	--	dB
	Single-ended input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	98	--	dB
THD+N	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-90	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-88	--	dB
Analogue Gain	--	-6	--	27	dB
Max Input Level	Differential input Mode ADC gain=0dB	--	0.56	--	Vrms
	Single-ended input Mode ADC gain=0dB	--	0.28	--	Vrms

3.8 BT Characteristics

3.8.1 Transmitter

Table 3-8-1 Transmitter characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Maximum RF Transmit Power	BR	--	10	13	dBm
Maximum RF Transmit Power	EDR Π/4 DQPSK EDR 8DPSK	--	10	--	dBm
Relative Transmit Power	EDR Π/4 DQPSK EDR 8DPSK	--	1	--	dB
Maximum RF Transmit Power	BLE-1Mbps	--	10	--	dBm
1σ of Maximum RF Transmit Power distribution	BR/EDR/BLE	--	2	--	dB

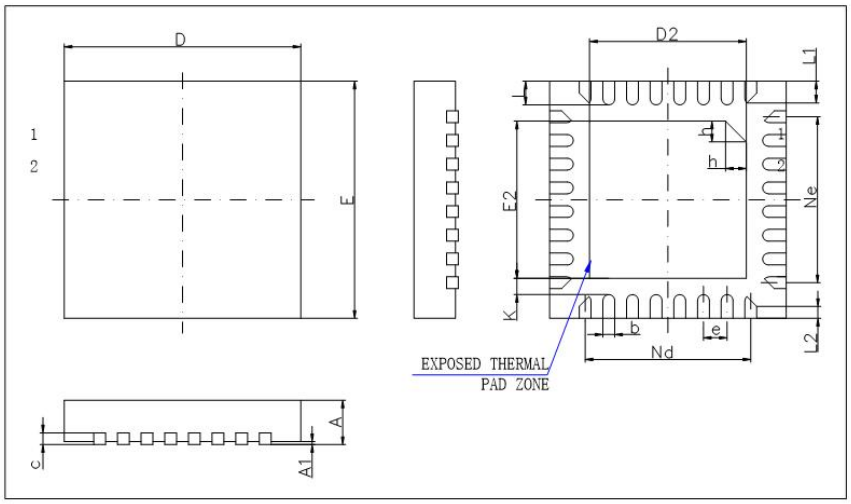
3.8.2 Receiver

Table 3-8-2 Receiver characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity	BR	--	-94	--	dBm
	EDR Π/4 DQPSK	--	-95	--	dBm
	EDR 8DPSK	--	-87	--	dBm
	BLE-1Mbps	--	-97	--	dBm
	BLE-2Mbps	--	-93	--	dBm
1σ of sensitivity distribution	BR/EDR/BLE	--	2	--	dB

4 Package Information

4.1 QFN32_4×4mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.80	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50	2.65	2.80
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.50	2.65	2.80
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F 载体尺寸 (mil)	112*112		

Figure 4-1 JL7106F Package

5 IC Marking Information

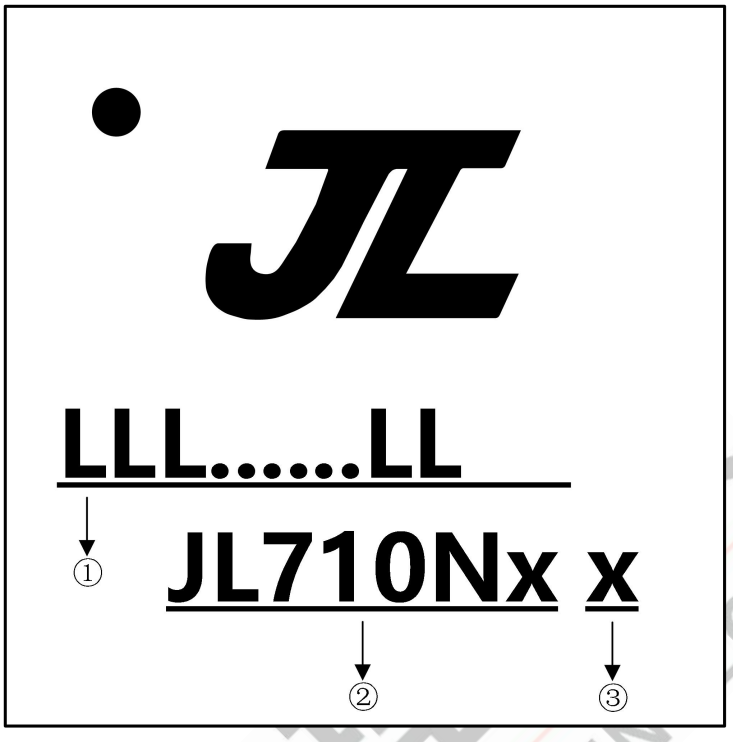


Figure 5-1 JL7106F Package Outline

① LLL.....LL Production Batch
② JL710Nx Chip Model
③ x Built-in flash size
4 4Mbit Flash
8 8Mbit Flash
6 16Mbit Flash

6 Solder-Reflow Condition

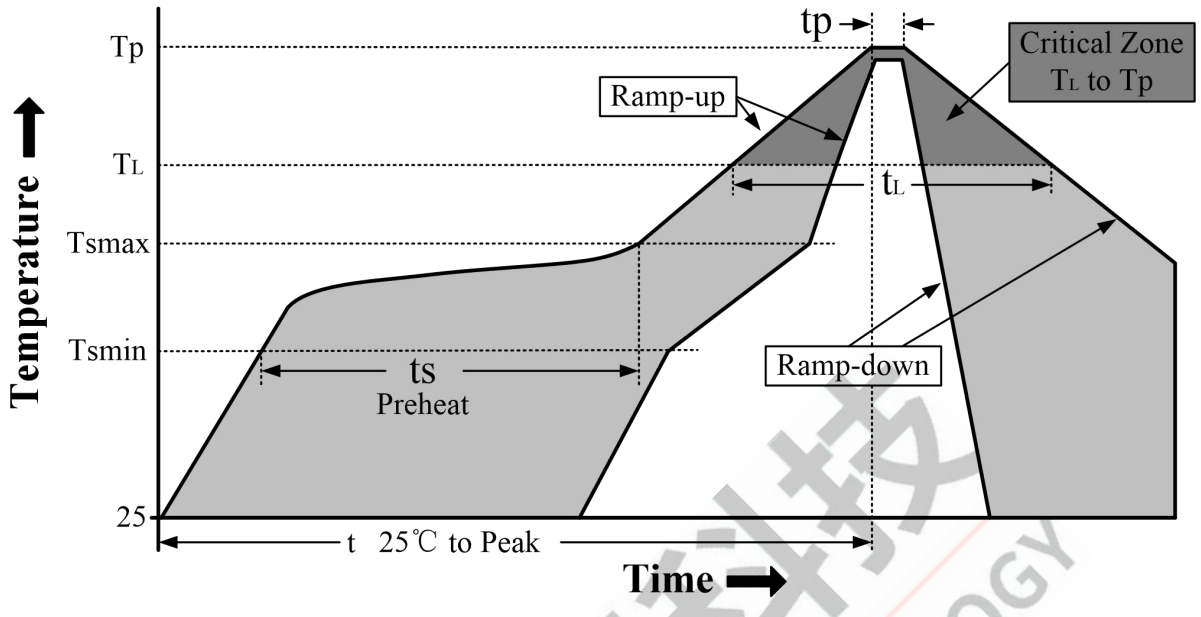


Figure 6-1 Classification Reflow Profile

Table 6-1 Classification Profiles

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min (T_{smin})	100℃	150℃
	Temperature Max (T_{smax})	150℃	200℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5℃ of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6℃/second max	6℃/second max
Time 25℃ to peak temperature		6 minutes max	8 minutes max

Note

1.All temperatures refer to topside of the package, measured on the package body surface

2.Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" and "user" maximum.

Table 6-2 SnPb Classification Temperature

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
≥2.5 mm	225 +0/-5℃	225 +0/-5℃

Table 6-3 Pb-free - Classification Temperature

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

Note

1.*Tolerance The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0℃.For example 260℃+0℃)at the rated MSL level.