PF8210 Dual Mode 2x3.2W Stereo Audio Amplifier with Anti-Clipping

Features

- Supply Voltage from 2.7V to 6.0V
- 3.2W@10% THD Output with a 4Ω Load at 5V Supply
- Anti-Clipping with Adaptive PWM Control
- High Efficiency
  - ✓ Up to 90% with 8Ω Load
  - ✓ Up to 87% with 4Ω Load
- Support Class AB Output
- One-wire Control
- Shutdown Current <1μA
- Superior Low Noise without Input
- EMI Suppressing by Soft-Driving
- Short Circuit Protection
- Thermal Shutdown
- Available in QFN3*3-16L Pb-Free Package

Description

The PF8210 is a stereo filter-less class-D amplifier with high SNR and differential input that eliminate noise. With an alternative option between Class-D and Class-AB output, which makes the device very ideal for efficiency-EMI compatible applications.

Features like higher than 90% efficiency and small PCB area make the PF8210 class-D amplifier ideal for portable devices. The filter-less architecture requires no external output filter, fewer external components, less PCB area and lower system costs, and simplifies application design.

Integrated APWM anti-clipping technology suppresses output automatically improving the sound quality and helping to protect the speakers.

With the soft-driving technology, the edge of the PWM at output stage is very flat which is very useful for EMI suppressing.

The PF8210 features short circuit protection, thermal shutdown and under voltage lock-out.

The PF8210 is available in QFN3*3-16L packages.

Application

- Flat Panel Display
- LCD Monitors and TVs
- Projectors / All-In-One Computers
- Portable / Active Speakers
- Portable DVD Players / Game Machines

Ordering Information

Part Number	Package	Top Mark	Quantity/ Reel
PF8210	QFN3*3-16L	T8210B XXXXXX	3000

PF8210 devices are Pb-free and RoHS compliant.

Typical Application

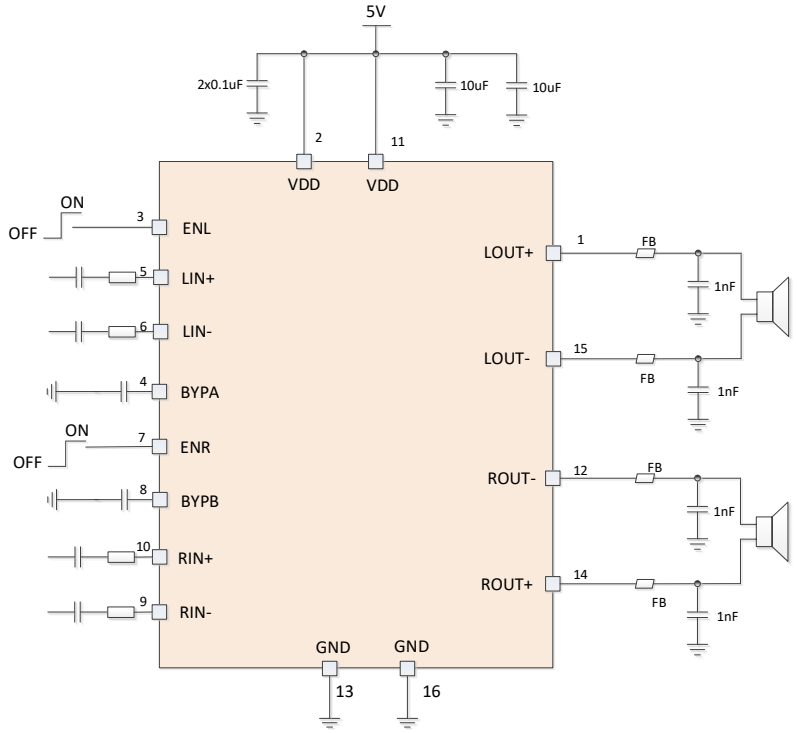


Fig-1: Typical Application Circuit

Block Diagram

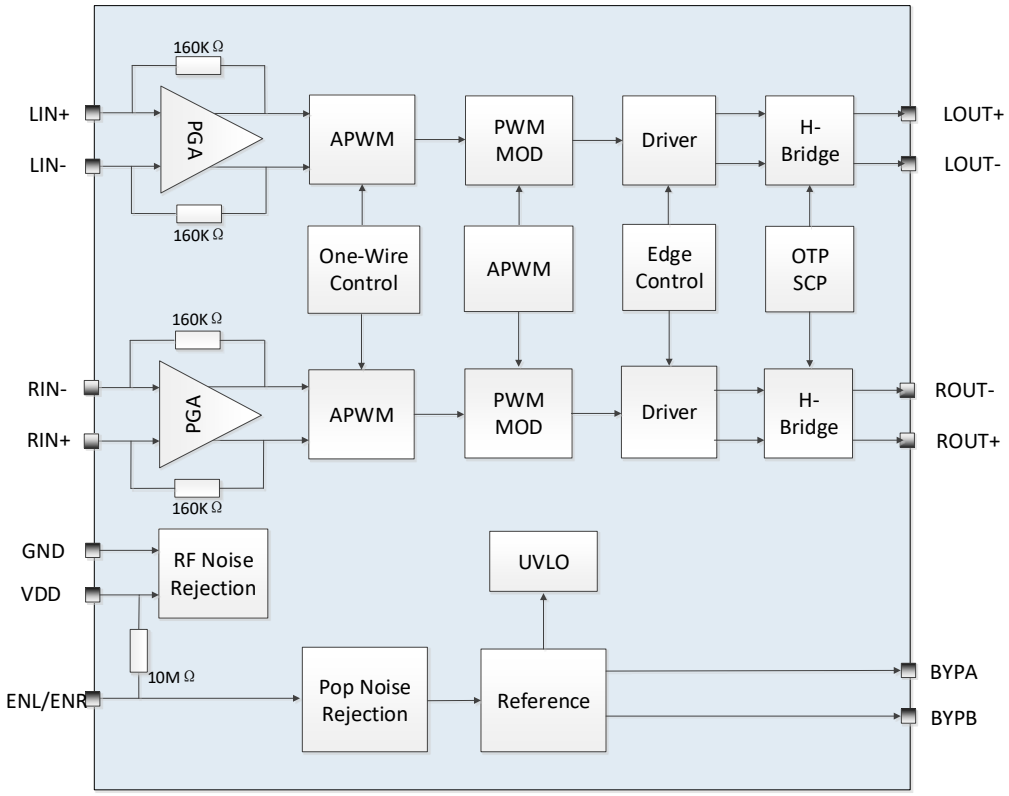


Fig-2: Block Diagram

Package & Pin Configuration

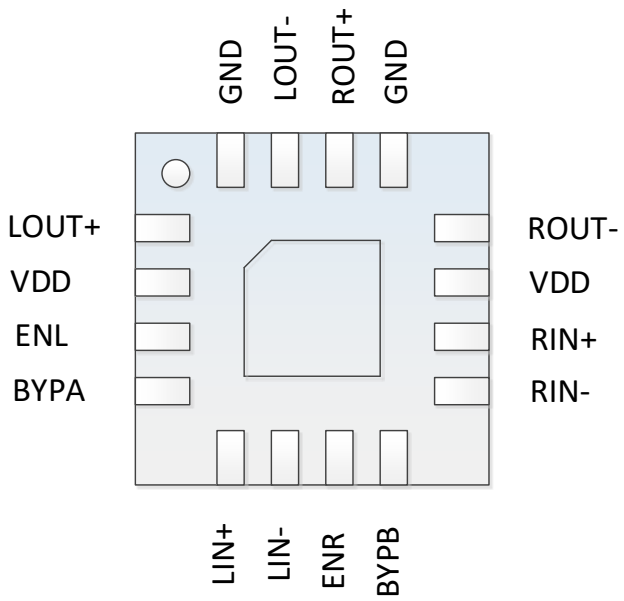


Fig-3: QFN3*3-16L (Top View)

Pin Functions

Pin Name	Pin Number	I/O/P	Description
LOUT+	1	O	Left Channel Positive BTL of Right Channel Power Amplifier
VDD	2	P	Power Supply
ENL	3	I	Control Terminal for Left Channel
BYPA	4	O	Internal Reference Voltage Bypass Pin 1; Connect a 1.0uF Capacitance from Thins Pin to GND
LIN+	5	I	Left channel Positive Differential Input
LIN-	6	I	Left channel Negative Differential Input
ENL	7	I	Control Terminal for Right Channel
BYPB	8	O	Internal Reference Voltage Bypass Pin 2; Connect a 1.0uF Capacitance from Thins Pin to GND
RIN-	9	I	Right channel Negative Differential Input
RIN+	10	I	Right channel Positive Differential Input
VDD	11	P	Power Supply
ROUT-	12	O	Right Channel Negative BTL of Right Channel Power Amplifier
GND	13	P	Ground
ROUT+	14	O	Right Channel Positive BTL of Right Channel Power Amplifier
LOUT-	15	O	Left Channel Negative BTL of Right Channel Power Amplifier
GND	16	P	Ground

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage	-0.3 to +6.5	V
INx/ENx	Input Voltage	-0.3 to V_{DD}+0.3	V
T_J	Junction Temperature	-55 to +150	°C
T_{STG}	Storage Temperature	-65 to +165	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These voltages represent the DC voltage plus peak AC waveform measured at the terminal of the device in all conditions.

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage	+3.0 to +6.0	V
T_A	Operating free-air temperature	-40 to +85	°C
T_J	Junction Temperature	-40 to +125	°C

ESD Rating

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model	±4000	V
V_{ESD_CDM}	Charge Device Model	±750	V

Electrical Characteristics

T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Class D Mode							
Po	Output Power	THD+N=10%, f=1kHz, R_L=4Ω	V_{DD}=5.0V		3.2		W
			V_{DD}=3.7V		1.75		
		THD+N=1%, f=1kHz, R_L =4Ω	V_{DD}=5.0V		2.6		W
			V_{DD}=3.7V		1.5		
		THD+N=10%, f=1kHz, R_L =8Ω	V_{DD}=5.0V		1.75		W
			V_{DD}=3.7V		0.95		
		THD+N=1%, f=1kHz, R_L =8Ω	V_{DD}=5.0V		1.50		W
			V_{DD}=3.7V		0.8		
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=5.0V, Po=0.25W	f=1kHz, R_L =8Ω		0.035		%
		V_{DD}=3.7V, Po=0.25W			0.04		
		V_{DD}=5.0V, Po=0.5W	f=1kHz, R_L =4Ω		0.04		%
		V_{DD}=3.7V, Po=0.5W			0.045		
PSRR	Power Supply Ripple Rejection	V_{DD}=5V, Inputs AC-Grounded	f=217Hz		-65		dB
			f=1kHz		-65		
SNR	Signal-to-Noise Ratio	V_{DD}=5V, THD=1%, f=1kHz	A-weighting		95		dB
Vn	Output Noise	Inputs AC-Grounded, G_V=6dB	No A-weighting		120		μV
			A-weighting		65		
G_V	Closed-loop Gain	V_{DD}= 5V			310K /Rin		V/V
fsw	Switching Frequency	V_{DD}= 5V			300		kHz
η	Efficiency	R_L=8Ω, THD=10%	f=1kHz		93		%
		R_L=4Ω, THD=10%			86		
I_Q	Quiescent Current	V_{DD}=5V	No Load		20		mA
Class AB Mode							
Po	Output Power	THD+N=10%, f=1kHz, R_L =4Ω	V_{DD}=5.0V		3		W
			V_{DD}=3.7V		1.7		
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=5.0V, Po=0.25W, R_L =8Ω	f=1kHz		0.25		%
		V_{DD}=3.7V, Po=0.25W, R_L =8Ω			0.2		
Vn	Output Noise	Inputs AC-Grounded, G_V=6dB	No A-weighting		60		μV
			A-weighting		110		
I_Q	Quiescent Current	V_{DD}=5V	No Load		18		mA

Electrical Characteristics

T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

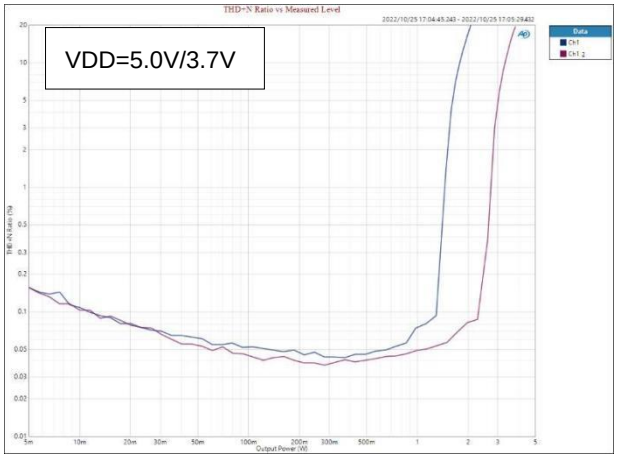
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
DC Parameters							
I_{SD}	Shutdown Current	V_{DD}=2.8V to 5.5V	ENx=0V			1	μA
R_{SDON}	Static Drain-to Source On-state Resistor	High Side + Low Side	V_{DD}=5.0V, I=500mA		355		mΩ
T_{ON}	Turn On Time	V_{DD}= 5V			30		ms
V_{OS}	Output Offset Voltage	Input AC-Ground, V_{DD}=5V			10		mV
V_{IH}	Input High Voltage	V_{DD}=5V		1.4			V
V_{IL}	Input Low Voltage	V_{DD}=5V				1.0	

Performance Characteristics

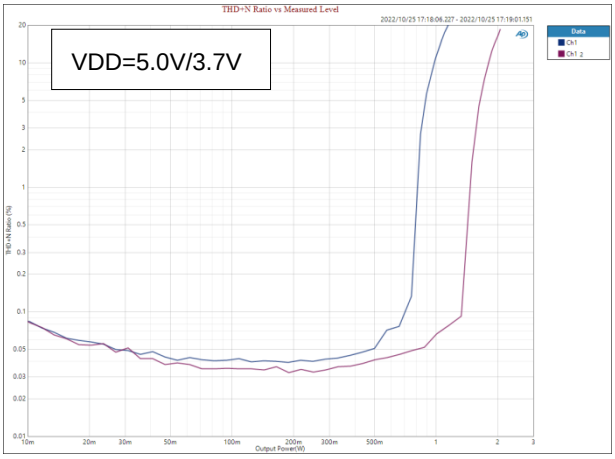
T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Class D Mode

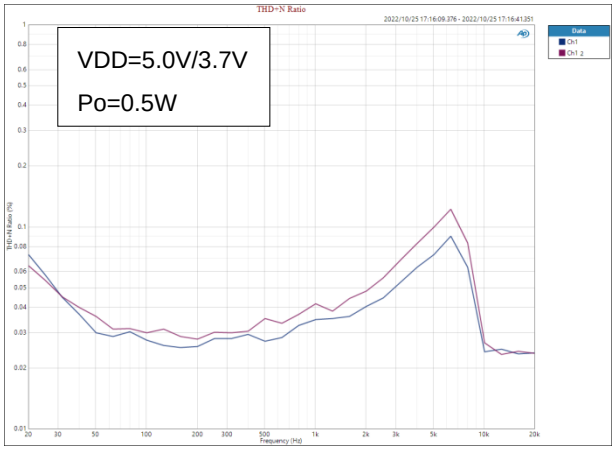
THD+N Vs. Output Power (R_L=4Ω)



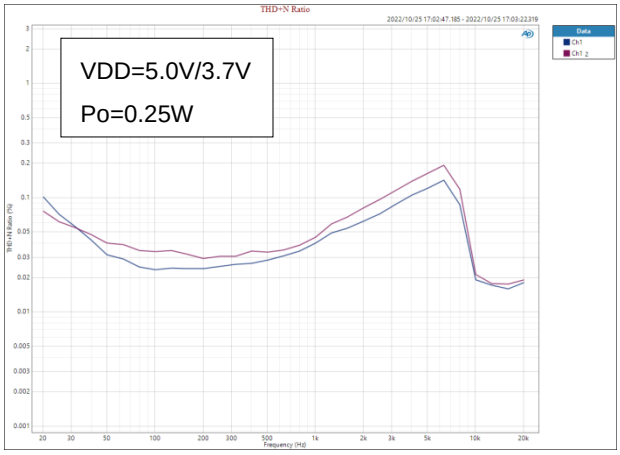
THD+N Vs. Output Power (R_L=8Ω)



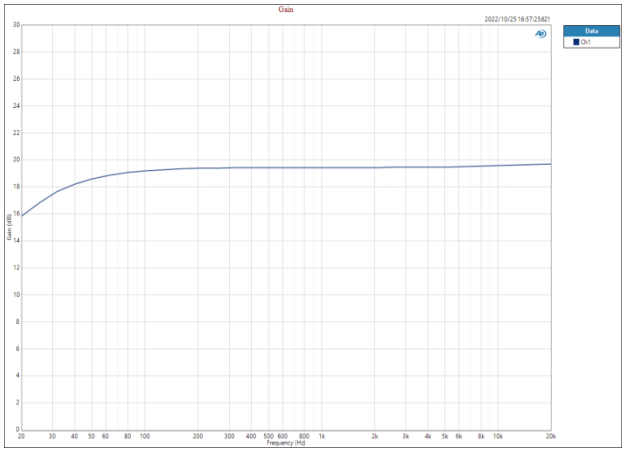
THD+N Vs. Frequency (RL=4Ω)



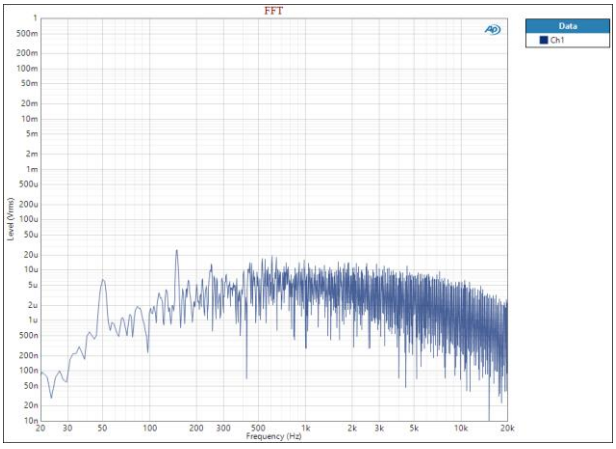
THD+N Vs. Frequency (RL=8Ω)



Frequency Response



Noise Floor

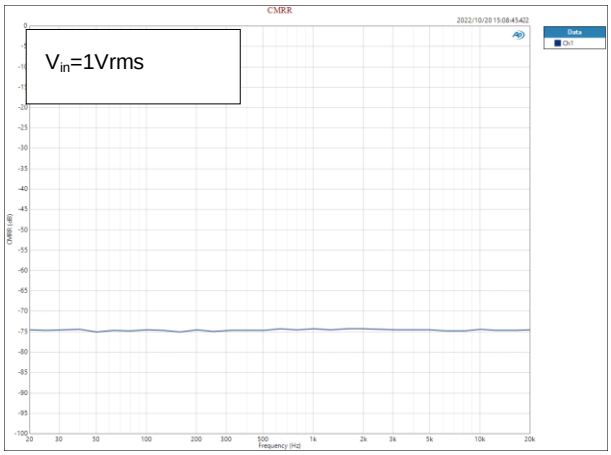


Performance Characteristics

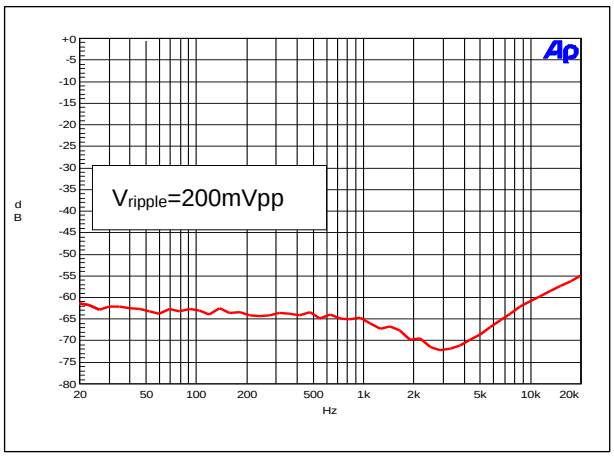
T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Class D Mode

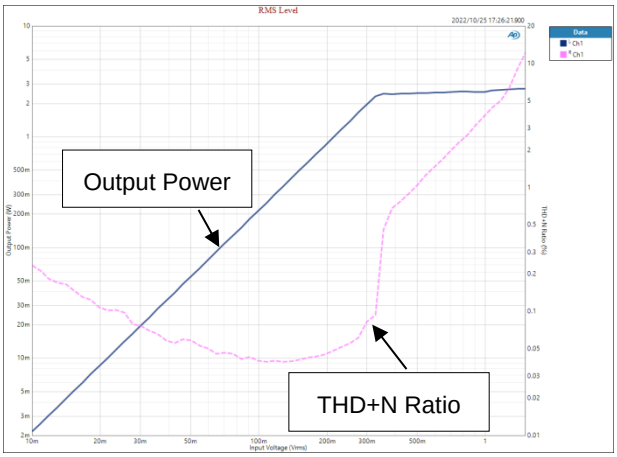
CMRR



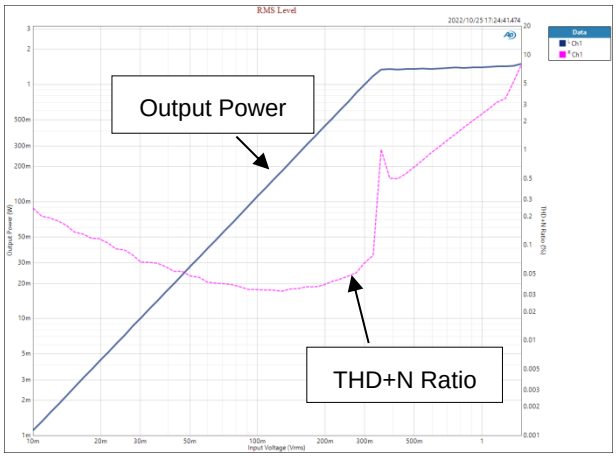
PSRR



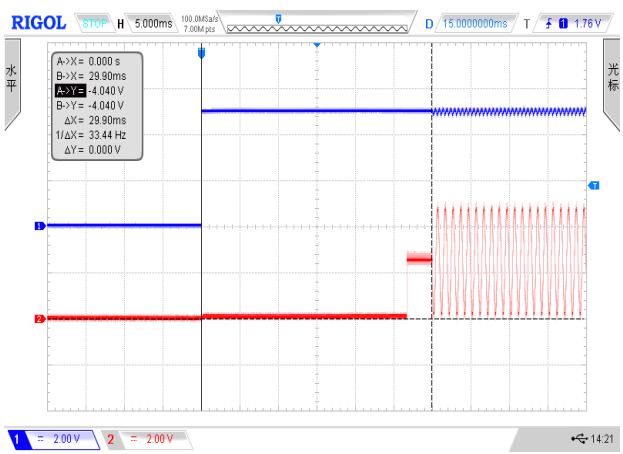
NCN1 Characteristics (RL=4Ω)



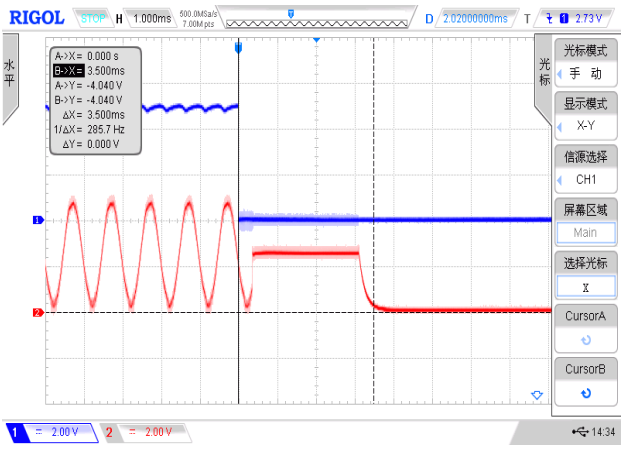
NCN1 Characteristics (RL=8Ω)



Start-up Response



Shutdown Response

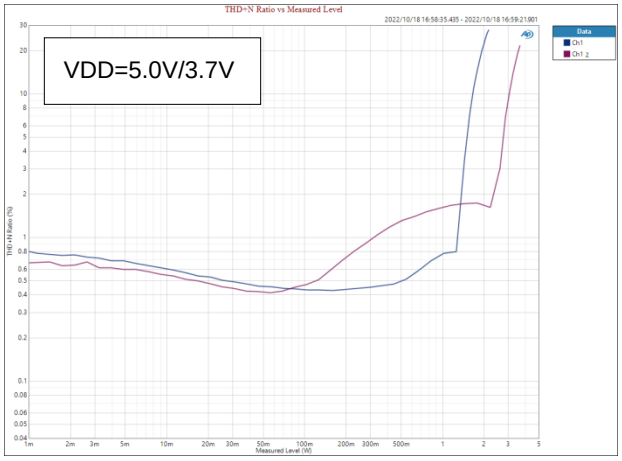


Performance Characteristics

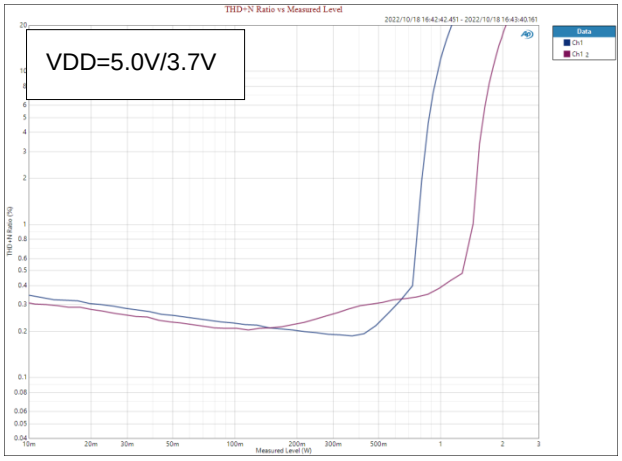
T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, unless otherwise noted.

Class AB Mode

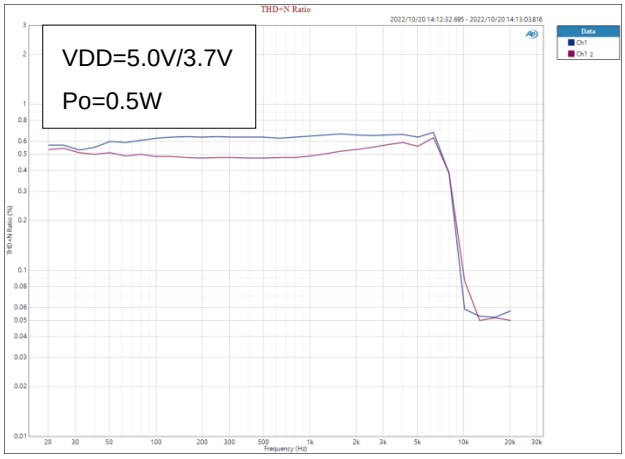
THD+N Vs. Output Power (RL=4Ω)



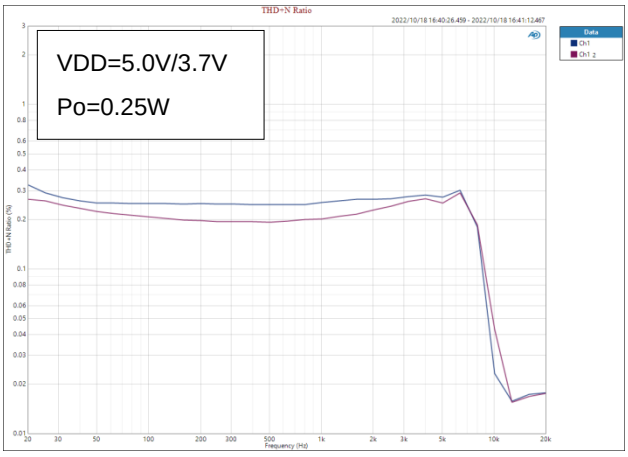
THD+N Vs. Output Power (RL=8Ω)



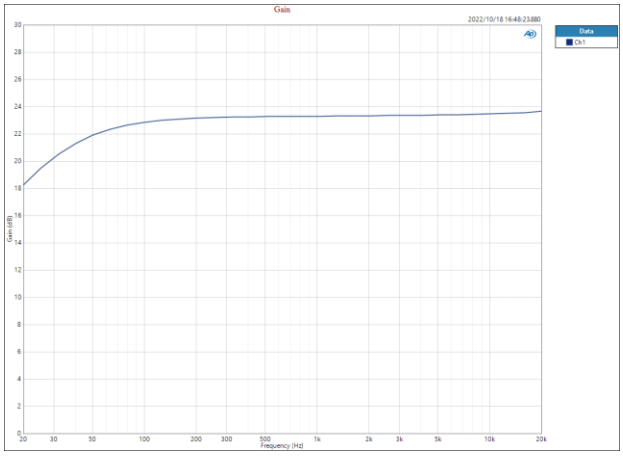
THD+N Vs. Frequency (RL=4Ω)



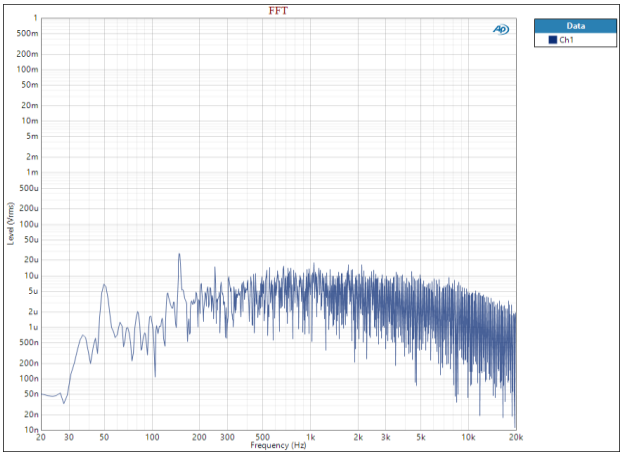
THD+N Vs. Frequency (RL=8Ω)



Frequency Response



Noise Floor



Application Information

Input Resistor (Ri) and Gain Setting

The input resistors (Ri) and feedback resistors (155kΩ refer to block diagram) internally set the gain of the amplifier according to the following equation.

$$Gain = \frac{2*155(\mathrm{k}\Omega)}{\mathrm{R}i(k\Omega)} \quad (\mathrm{V/V})$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%. Place the input resistors very close to the PF8210 to limit noise injection on the high-impedance nodes. For optimal performance, the gain should be set to 2V/V or lower. Lower gain allows the PF8210 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$\mathrm{f_C} = \frac{1}{(2\pi \mathrm{RiCi})}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 150kΩ and the specification calls for a flat bass response are down to 150Hz. Equation is reconfigured as followed:

$$\mathrm{Ci} = \frac{1}{(2\pi \mathrm{Ri f_c})}$$

When input resistance variation is considered, the Ci is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at VDD/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (CS)

The PF8210 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low Equivalent-Series-Resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to the device VDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Analog Reference Bypass Capacitor (C_{BYP})

Analog Reference Bypass Capacitor C_{BYP} is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N. A 1μF capacitance is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 3. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

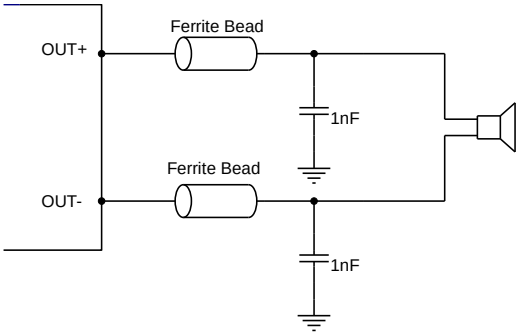


Figure 3: Ferrite Bead Filter to Reduce EMI

Under Voltage Lock-out (UVLO)

The PF8210 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.4V or below, the PF8210 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when VDD higher than 2.5V.

Short Circuit Protection (SCP)

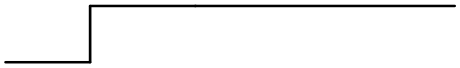
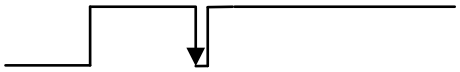
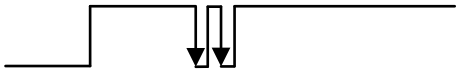
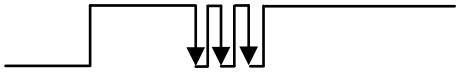
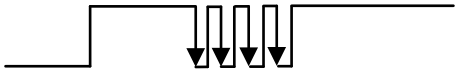
The PF8210 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. When a short circuit occurs, the device immediately goes into shutdown state. Once the short is removed, the device will be reactivated.

EN Pin Function

EN pin features multi functions.

To achieve high sound quality, the PF8210 works at non-clipping mode 1(NCN1) once pull EN pin voltage to high (power on default), and the chip works at other modes when the serial

pulses(one-wire-control) applied to the EN pin. Below table shows the PF8210 behaviors versus EN Pin waveform.

EN Waveform	PF8210 Behavior	Note
	Class D with NCN1	Power on default
	Class D with NCN1	One falling edge
	Class D with NCN2	Two falling edges
	Class D without NCN	Three falling edges
	Class AB without NCN	Four falling edges

In order to reduce power consumption while not in use, the PF8210 contains shutdown circuitry amplifier off when logic low(t_{SD}>10ms) is placed on the EN pin. By switching the EN pin connected to logic low, the PF8210 supply current draw will be minimized in idle mode.

Timing of the one-wire-control for the EN:

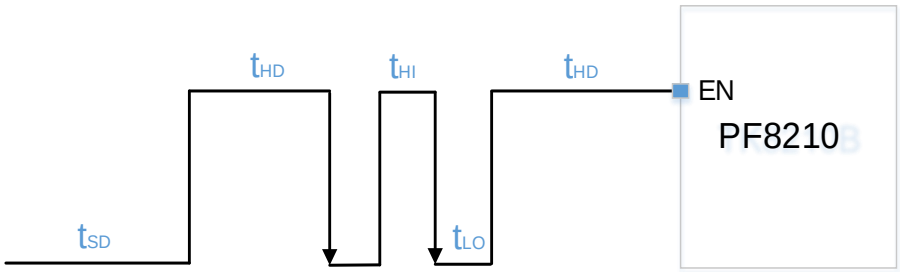


Figure 4: EN Pin Timing

a, Hold time t_{HD}>10ms

b, High level time: 20μs <t_{HI}<100μs;

c, Low level time: 20μs <t_{HI}<100μs;

d, Chips shutdown when the t_{LO} more than 10ms(t_{SD});

Soft-Clipping Output (NCN)

The PF8210 provides auto non-clipping control, and the range is from 24dB (Rin=20kΩ) to 9dB. When the output reaches the maximum power value, the internal Programmable Gain Amplifier (PGA) will decrease the gain to prevent the output waveform clipping. This feature prevents the audio sound to be distorted and protects speaker damage from being overstressed. Using the EN pin to set the non-clipping Mode 1(NCN1:20ms attack time) and non-clipping Mode 2(NCN2:40ms attack time).

Over Temperature Protection (OTP)

Thermal protection on the PF8210 prevents the device from damage when the internal die temperature exceeds 150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 40°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

POP and Click Circuitry

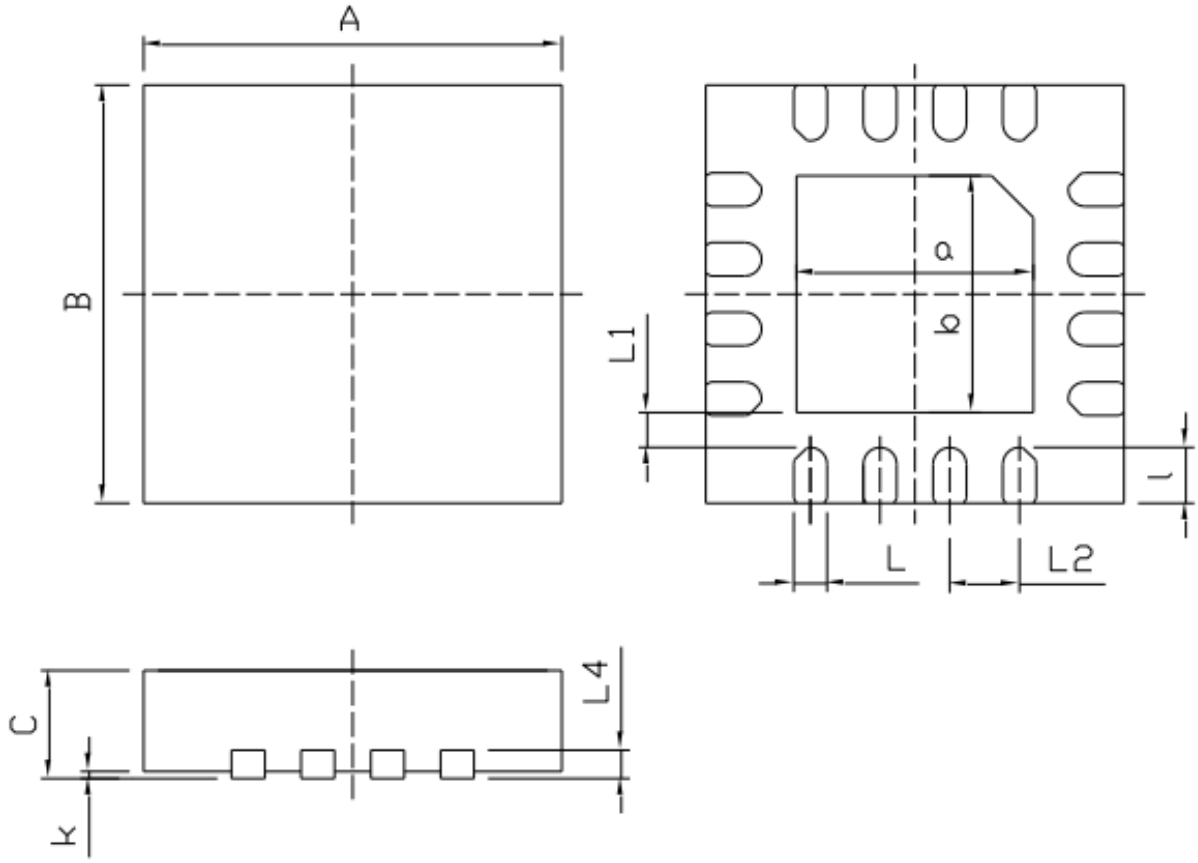
The PF8210 contains circuitry to minimize turn-on and turn-off transients or “click and pops”, where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 VDD. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Class AB Mode

The chip will operation at Class AB mode to avoid any RF interference when apply serial pulse applied to the EN pin. (Please see the EN Pin Function)

Package Information

Package: QFN3*3-16L:



Dimensions In Millimeterer			
Symbol	MIN	TYP	MAX
A	2.90	3.00	3.10
B	2.90	3.00	3.10
C	0.70	0.75	0.80
L	0.18	0.24	0.30
L1	-	0.25	-
L2	-	0.50	-
L4	-	0.203	-
a	1.60	1.70	1.80
b	1.60	1.70	1.80
k	0.00	0.02	0.05
l	0.30	0.40	0.50