

# **AD6973M Datasheet**

**Zhuhai Jieli Technology Co.,LTD**

**Version: 1.3**

**Date: 2025.01.15**

**Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.**

# AD6973M Features

## CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64 Vectored interrupts
- 8 Levels interrupt priority

## DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single/Dual analog/digital MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

## Audio Codec

- Two channels 24-bit DAC, SNR >= 101dB
- Two channels 24-bit ADC , SNR >= 85dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- One channel Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

## Bluetooth

- Compliant with Bluetooth V6.0+BR+EDR+BLE specification

(DN Q334307)

- Meet class2 and class3 transmitting power requirement
- Support GFSK and  $\pi/4$  DQPSK all packet types
- Provides maximum +8dbm transmitting power
- receiver with minimum -94dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smpt\att\gap\gatt\rfcomm\sdpl2cap profile
- a2dp 1.4\avctp 1.4\avdtp 1.3\ avrcp 1.6.3\hfp 1.9\spp 1.2\rfcomm 1.2\pnp 1.3\hid 1.1.1\sdpcore 6.0\l2cap core 6.0

## Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, support DMA mode
- One hardware IIC interface supports host and device mode
- Two Built-in low power Cap Sense Keys
- Built-in Cap Sense Key controller
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

## PMU

- Low voltage LDO and DC-DC for internal digital and analog circuit supply
- 2uA current consumption in the soft-off mode
- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.5V
- VDDIO is 2.2V to 3.4V

## Packages

- QFN20(3mm\*3mm)

### Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

### Applications

- 2.4G wireless MIC



### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

# 1、 Pin Definition

## 1.1 Pin Assignment

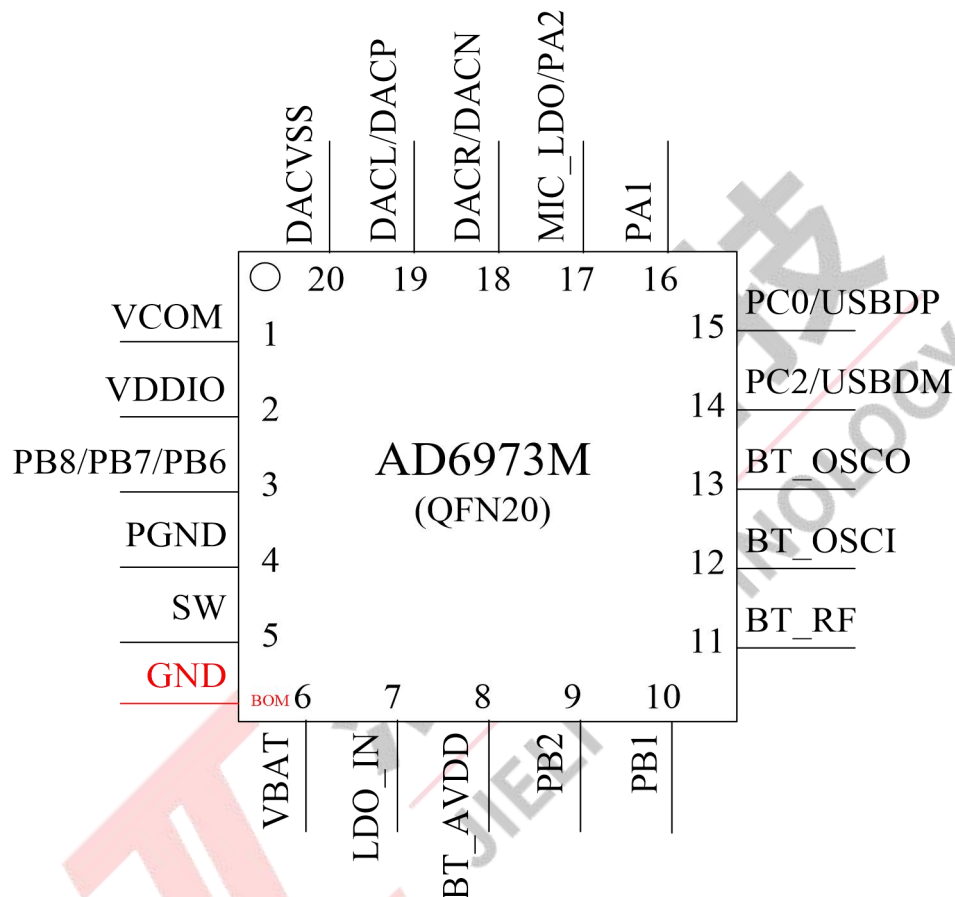


Figure 1-1 AD6973M Package Diagram

## 1.2 Pin Description

Table 1-1 AD6973M Pin Description

| PIN NO. | Name    | I/O Type | Drive (mA) | Function       | Other Function                                                                                                                                           |
|---------|---------|----------|------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | VCOM    | P        | /          |                | DAC reference voltage                                                                                                                                    |
| 2       | VDDIO   | P        | /          |                | IO Power 3.3v                                                                                                                                            |
| 3       | PB8     | I/O      | 8/24       | GPIO           | MIC1: MIC1 Input Channel;<br>UART0RXB: Uart0 Data Input(B);<br>CAP4: Timer4 Capture;                                                                     |
|         | PB7     | I/O      | 8/24       | GPIO           | MIC_BIAS1: MIC1 Bias Output;<br>UART0TXB: Uart0 Data Output(B);                                                                                          |
|         | PB6     | I/O      | 8/24       | GPIO           | UART1RXA: Uart1 Data Input(A);<br>PWM2: Timer2 PWM Output;<br>ADC9: ADC Input Channel 9;<br>Touch7: Touch Input Channel 7;                               |
| 4       | PGND    | P        | /          |                | DCDC Ground                                                                                                                                              |
| 5       | SW      | P        | /          | DCDC output    | DCDC switch output, connected to inductor                                                                                                                |
| 6       | VBAT    | P        | /          |                | connect to battery                                                                                                                                       |
| 7       | LDO_IN  | P        | /          |                | Charge Power Input;<br>UART0TXC: Uart0 Data Output(C);<br>UART0RXC: Uart0 Data Input(C);<br>PWM3: Timer3 PWM Output;<br>CAP1: Timer1 Capture;            |
| 8       | BT_AVDD | P        | /          |                | BT Power                                                                                                                                                 |
| 9       | PB2     | I/O      | 8/24       | GPIO           | UART2RXC: Uart2 Data Input(C);<br>SPI2DOC: SPI2 Data Out(C);<br>CAP5: Timer5 Capture;<br>ADC7: ADC Input Channel 7;<br>LP_TH1: Low Power Touch Channel 1 |
| 10      | PB1     | I/O      | 8/24       | GPIO (pull up) | Long Press Reset;<br>SPI2CLKC: SPI2 Clk(C);<br>UART2TXC: Uart2 Data Output(C)<br>ADC6: ADC Input Channel 6;<br>LP_TH0: Low Power Touch Channel 0         |
| 11      | BT_RF   | /        | /          |                | BT Antenna                                                                                                                                               |
| 12      | BT_OSCI | I        | /          |                | BTOSC In                                                                                                                                                 |
| 13      | BT_OSCO | O        | /          |                | BTOSC Out                                                                                                                                                |
| 14      | PC2     | I/O      | 8/24       |                | IIC_SCL_C: IIC SCL(C);                                                                                                                                   |

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

|    |           |     |      |                   |                                                                                                                                                                |
|----|-----------|-----|------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |           |     |      |                   | UART0TXD: Uart0 Data Output(D);<br>TMR1: Timer1 Clock Input;                                                                                                   |
|    | USBDM     | I/O | 4    | USB Negative Data | UART1RXD: Uart1 Data Input(D);<br>IIC_SDA_A: IIC SDA(A);<br>ADC11: ADC Input Channel 11;                                                                       |
| 15 | USBDP     | I/O | 4    | USB Positive Data | UART1TXD: Uart1 Data Output(D);<br>IIC_SCL_A: IIC SCL(A);<br>ADC10: ADC Input Channel 10;                                                                      |
|    | PC0       | I/O | 8    | GPIO              | UART1TXB: Uart1 Data Output(B);                                                                                                                                |
| 16 | PA1       | I/O | 8/24 | GPIO              | MIC0: MIC0 Input Channel ;<br>PWM0: Timer0 PWM Output;<br>UART1TXC: Uart1 Data Output(C);                                                                      |
| 17 | MIC_LDO   | P   | /    |                   | MIC Power                                                                                                                                                      |
|    | PA2       | I/O | 8/24 | GPIO              | ALNK_MCLK(A): ALNK Master Clock(A);<br>MIC_BIAS0: MIC0 Bias Output;<br>MIC0_N: Different MIC0 Negative<br>CAP3: Timer3 Capture;<br>UART1RXC: Uart1 Data In(C); |
| 18 | DACR/DACN | O   | /    |                   | DAC Right Channel<br>Different DAC Negative Channel                                                                                                            |
| 19 | DACL/DACP | O   | /    |                   | DAC Left Channel<br>Different DAC Positive Channel                                                                                                             |
| 20 | DACVSS    | P   | /    |                   | Analog Ground                                                                                                                                                  |

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 2、Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 2-1

| Symbol             | Parameter             | Min  | Max  | Unit |
|--------------------|-----------------------|------|------|------|
| Tamb               | Ambient Temperature   | -40  | +85  | °C   |
| Tstg               | Storage temperature   | -65  | +150 | °C   |
| VBAT               | Supply Voltage        | -0.3 | 4.5  | V    |
| LDO_IN             | Charger Voltage       | -0.3 | 6    | V    |
| V <sub>3.3IO</sub> | 3.3V IO Input Voltage | -0.3 | 3.6  | V    |

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

### 2.2 PMU Characteristics

Table 2-2

| Symbol      | Parameter              | Min | Typ | Max | Unit | Test Conditions           |
|-------------|------------------------|-----|-----|-----|------|---------------------------|
| VBAT        | Voltage Input          | 2.2 | 3.7 | 4.2 | V    |                           |
| LDO_IN      | Charger supply Voltage | 4.5 | 5.0 | 5.5 | V    |                           |
| Normal mode |                        |     |     |     |      |                           |
| VDDIO       | Voltage output         | —   | 3.0 | —   | V    | VBAT = 4.2V, 10mA loading |
|             | Loading current        | —   | —   | 100 | mA   | VDDIO=3V@VBAT = 4.2V      |
| BT_AVDD     | Voltage output         | —   | 1.3 | —   | V    | VDDIO=3.0V, 10mA loading  |
|             | Loading current        | —   | —   | 60  | mA   | BT_AVDD=1.25V@VDDIO=3.0v  |
| LP mode     |                        |     |     |     |      |                           |
| VDDIO       | Loading current        | —   | —   | 5   | mA   | VDDIO=3V@VBAT = 4.2V      |

### 2.3 Battery Charge

Table 2-3

| Symbol              | Parameter            | Min  | Typ  | Max  | Unit | Test Conditions |
|---------------------|----------------------|------|------|------|------|-----------------|
| LDO_IN              | Charge Input Voltage | 4.5  | 5    | 5.5  | V    | —               |
| V <sub>Charge</sub> | Charge Voltage       | 4.15 | 4.2  | 4.25 | V    | LDO_IN>4.5V     |
|                     |                      | 4.30 | 4.35 | 4.40 | V    | LDO_IN>4.65V    |

|                     |                        |    |    |     |    |                                     |
|---------------------|------------------------|----|----|-----|----|-------------------------------------|
| $I_{\text{Charge}}$ | Charge Current         | 20 |    | 200 | mA | Charge current at fast charge mode  |
| $I_{\text{Trikl}}$  | Trickle Charge Current | 20 | 45 | 70  | mA | $V_{\text{BAT}} < V_{\text{Trikl}}$ |

## 2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

| IO input characteristics  |                           |                         |     |                         |      |                                 |
|---------------------------|---------------------------|-------------------------|-----|-------------------------|------|---------------------------------|
| Symbol                    | Parameter                 | Min                     | Typ | Max                     | Unit | Test Conditions                 |
| $V_{\text{IL}}$           | Low-Level Input Voltage   | -0.3                    | —   | $0.3 * V_{\text{DDIO}}$ | V    | $V_{\text{DDIO}} = 3.3\text{V}$ |
| $V_{\text{IH}}$           | High-Level Input Voltage  | $0.7 * V_{\text{DDIO}}$ | —   | $V_{\text{DDIO}} + 0.3$ | V    | $V_{\text{DDIO}} = 3.3\text{V}$ |
| IO output characteristics |                           |                         |     |                         |      |                                 |
| $V_{\text{OL}}$           | Low-Level Output Voltage  | —                       | —   | 0.33                    | V    | $V_{\text{DDIO}} = 3.3\text{V}$ |
| $V_{\text{OH}}$           | High-Level Output Voltage | 2.7                     | —   | —                       | V    | $V_{\text{DDIO}} = 3.3\text{V}$ |

## 2.5 Internal Resistor Characteristics

Table 2-5

| Port                         | General Output | High Drive | Internal Pull-Up Resistor | Internal Pull-Down Resistor | Comment                                                                                                                     |
|------------------------------|----------------|------------|---------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| PA1, PB1, PB2, PB6, PB8, PC2 | 8mA            | 24mA       | 10K                       | 10K                         | 1、PB1 default pull up<br>2、USBDM & USBDP default pull down<br>3、internal pull-up/pull-down resistance   accuracy $\pm 20\%$ |
| PC0                          | 8mA            | —          | 10K                       | 10K                         |                                                                                                                             |
| USBDP                        | 4mA            | —          | 1.5K                      | 15K                         |                                                                                                                             |
| USBDM                        | 4mA            | —          | 180K                      | 15K                         |                                                                                                                             |

## 2.6 DAC Characteristics

Table 2-6

| Parameter          | Min | Typ  | Max | Unit             | Test Conditions                                      |
|--------------------|-----|------|-----|------------------|------------------------------------------------------|
| Frequency Response | 20  | —    | 20K | Hz               | 1KHz/0dB<br>10Kohm loading<br>With A-Weighted Filter |
| THD+N              | —   | -80  | —   | dB               |                                                      |
| S/N                | —   | 101  | —   | dB               |                                                      |
| Crosstalk          | —   | -80  | —   | dB               |                                                      |
| Output Swing       | —   | 0.45 | —   | V <sub>rms</sub> |                                                      |
| Dynamic Range      | —   | 90   | —   | dB               | 1KHz/-60dB                                           |

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

|                  |   |    |    |    |                                          |
|------------------|---|----|----|----|------------------------------------------|
|                  |   |    |    |    | 10Kohm loading<br>With A-Weighted Filter |
| DAC Output Power | — | 20 | 30 | mW | 16ohm loading                            |

## 2.7 ADC Characteristics

Table 2-7

| Parameter     | Min | Typ | Max | Unit | Test Conditions                          |
|---------------|-----|-----|-----|------|------------------------------------------|
| Dynamic Range |     | 85  |     | dB   | Fsample=44.1kHz<br>Fin=1KHz 2mVpp Input  |
| S/N           | —   | 85  | —   | dB   | Fsample=44.1kHz<br>Fin=1KHz 1.2Vpp Input |
| THD+N         | —   | -60 | —   | dB   |                                          |
| Crosstalk     | —   | -80 | —   | dB   |                                          |

## 2.8 BT Characteristics

### 2.8.1 Transmitter

#### Basic Data Rate

Table 2-8

| Parameter              | Min   | Typ | Max | Unit | Test Conditions                             |
|------------------------|-------|-----|-----|------|---------------------------------------------|
| RF Transmit Power      |       | 6   | 8   | dBm  | 25°C,<br>Power Supply<br>VBAT=5V<br>2441MHz |
| RF Power Control Range |       | 20  |     | dB   |                                             |
| 20dB Bandwidth         |       | 950 |     | KHz  |                                             |
| Adjacent Channel       | +2MHz | -40 |     | dBm  |                                             |
|                        | -2MHz | -38 |     | dBm  |                                             |
| Transmit Power         | +3MHz | -44 |     | dBm  |                                             |
|                        | -3MHz | -35 |     | dBm  |                                             |

#### Enhanced Data Rate

Table 2-9

| Parameter                            | Min       | Typ | Max | Unit | Test Conditions                             |
|--------------------------------------|-----------|-----|-----|------|---------------------------------------------|
| Relative Power                       |           | -1  |     | dB   | 25°C,<br>Power Supply<br>VBAT=5V<br>2441MHz |
| $\pi/4$ DQPSK<br>Modulation Accuracy | DEVM RMS  | 6   |     | %    |                                             |
|                                      | DEVM 99%  | 10  |     | %    |                                             |
|                                      | DEVM Peak | 15  |     | %    |                                             |
| Adjacent Channel<br>Transmit Power   | +2MHz     | -40 |     | dBm  |                                             |
|                                      | -2MHz     | -38 |     | dBm  |                                             |
|                                      | +3MHz     | -44 |     | dBm  |                                             |
|                                      | -3MHz     | -35 |     | dBm  |                                             |

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 2.8.2 Receiver

### Basic Data Rate

Table 2-10

| Parameter                                  |       | Min | Typ | Max | Unit | Test Conditions                             |
|--------------------------------------------|-------|-----|-----|-----|------|---------------------------------------------|
| Sensitivity                                |       |     | -92 |     | dBm  | 25°C,<br>Power Supply<br>VBAT=5V<br>2441MHz |
| Co-channel Interference Rejection          |       |     | -13 |     | dB   |                                             |
| Adjacent Channel<br>Interference Rejection | +1MHz |     | +5  |     | dB   |                                             |
|                                            | -1MHz |     | +2  |     | dB   |                                             |
|                                            | +2MHz |     | +37 |     | dB   |                                             |
|                                            | -2MHz |     | +36 |     | dB   |                                             |
|                                            | +3MHz |     | +40 |     | dB   |                                             |
|                                            | -3MHz |     | +35 |     | dB   |                                             |

### Enhanced Data Rate

Table 2-11

| Parameter                                  |       | Min | Typ | Max | Unit | Test Conditions                             |
|--------------------------------------------|-------|-----|-----|-----|------|---------------------------------------------|
| Sensitivity                                |       |     | -94 |     | dBm  | 25°C,<br>Power Supply<br>VBAT=5V<br>2441MHz |
| Co-channel Interference Rejection          |       |     | -13 |     | dB   |                                             |
| Adjacent Channel<br>Interference Rejection | +1MHz |     | +5  |     | dB   |                                             |
|                                            | -1MHz |     | +2  |     | dB   |                                             |
|                                            | +2MHz |     | +37 |     | dB   |                                             |
|                                            | -2MHz |     | +36 |     | dB   |                                             |
|                                            | +3MHz |     | +40 |     | dB   |                                             |
|                                            | -3MHz |     | +35 |     | dB   |                                             |

## 2.9 ESD Protection

| Parameter           | Typ.       | Test pin       | Reference standard     |
|---------------------|------------|----------------|------------------------|
| Human Body Mode     | ± 4KV      | All pins       | JEDEC EIA/JESD22-A114  |
| Machine Mode        | ± 200V     | All pins       | JEDEC EIA/JESD22-A115  |
| Charge Device Model | ± 1KV      | All pins       | JEDEC EIA/JESD22-C101F |
| Latch up            | ± 200mA    | All GPIO pins  | JEDEC STANDARD NO.78E  |
|                     | 1.5xVopmax | All power pins |                        |

Note : 1.5xVopmax = 1.5 times maximum operating voltage

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 QFN20\_3.0x3.0

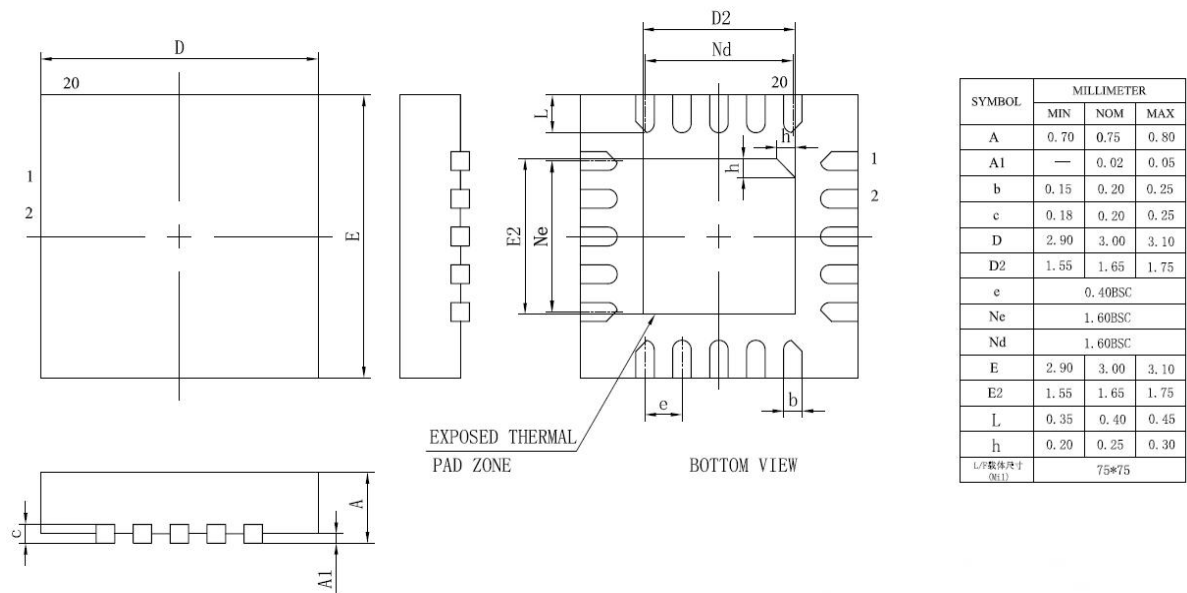


Figure 3-1 AD6973M Package

## 4、Solder-Reflow Condition

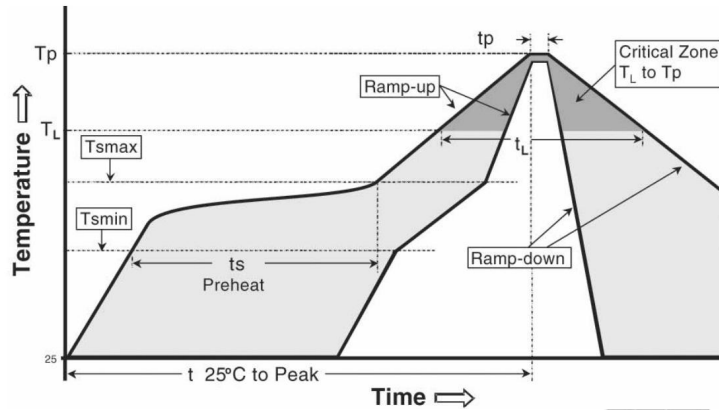


Figure 5-1 Classification Reflow Profile

### Classification Profiles

Table 5-1

| Profile Feature                                                      |                                                  | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|----------------------------------------------------------------------|--------------------------------------------------|-------------------------|------------------|
| Preheat<br>/Soak                                                     | Temperature Min ( $T_{smin}$ )                   | 100°C                   | 150°C            |
|                                                                      | Temperature Max ( $T_{smax}$ )                   | 150°C                   | 200°C            |
|                                                                      | Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ ) | 60-120 seconds          | 60-180 seconds   |
| Average ramp-up rate ( $T_{smax}$ to $T_p$ )                         |                                                  | 3°C/second max          | 3°C/second max   |
| Liquidous temperature ( $T_L$ )                                      |                                                  | 183°C                   | 217°C            |
| Time ( $t_L$ ) maintained above $T_L$                                |                                                  | 60-150 seconds          | 60-150 seconds   |
| Peak package body temperature ( $T_p$ )                              |                                                  | See Table 5-2           | See Table 5-3    |
| Time within 5°C of actual<br>Peak Temperature ( $t_p$ ) <sup>2</sup> |                                                  | 10-30 seconds           | 20-40 seconds    |
| Ramp-down rate ( $T_p$ to $T_L$ )                                    |                                                  | 6°C/second max          | 6°C/second max   |
| Time 25°C to peak temperature                                        |                                                  | 6 minutes max           | 8 minutes max    |

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature ( $t_p$ ) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

### SnPb - Classification Temperature

Table 5-2

| Package<br>Thickness | Volume mm <sup>3</sup><br>< 350 | Volume mm <sup>3</sup><br>≥ 350 |
|----------------------|---------------------------------|---------------------------------|
| <2.5 mm              | 240 +0/-5°C                     | 225 +0/-5°C                     |
| ≥2.5 mm              | 225 +0/-5°C                     | 225 +0/-5°C                     |

### Pb-free - Classification Temperature

Table 5-3

| Package<br>Thickness | Volume mm <sup>3</sup><br>< 350 | Volume mm <sup>3</sup><br>350 - 2000 | Volume mm <sup>3</sup><br>> 2000 |
|----------------------|---------------------------------|--------------------------------------|----------------------------------|
| < 1.6mm              | 260°C                           | 260°C                                | 260°C                            |
| 1.6 mm - 2.5mm       | 260°C                           | 250°C                                | 245°C                            |

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

|         |      |      |      |
|---------|------|------|------|
| > 2.5mm | 250℃ | 245℃ | 245℃ |
|---------|------|------|------|



## 5、Revision History

| Date       | Revision | Description                          |
|------------|----------|--------------------------------------|
| 2023.05.24 | V1.0     | Initial Release                      |
| 2024.08.16 | V1.1     | Update DAC Characteristics           |
| 2024.08.26 | V1.2     | Update AD6973M BT_Features           |
| 2025.01.15 | V1.3     | Update Bluetooth Vision and profiles |



### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.