AC7072A Datasheet

Zhuhai Jieli Technology Co.,LTD

Version 1.1

Date 2025.01.17

Revision History

Date	Revision	Description
2024.12.16	V1.0	Initial Release.
2025.01.17	V1.1	1.Upgrade the Bluetooth version to 6.0. 2.Modify the parameters of the Class-D Speaker and Audio ADC.

Table of Contents

AC7072A Features

SYSTEM

- 32bit Dual-Issue DSP 288MHz
- On-chip SRAM 284kbyte
- With I-cache and D-cache
- With IEEE754 Single precision FPU
- With MATH coprocessor
- Support EMU / MPU
- Support MMU
- Built-In Flash
- Support Built-In PSRAM
- 24MHz crystal oscillator
- Internal RC oscillator, PLL

DSP Audio Processing

- SBC/AAC/CVSD/mSBC codec
- mSBC voice codec supported for BT phone
- PLC for voice processing
- Single MIC ENC
- Multi-band DRC
- Multi-band EQ

Audio

- 1 x Class-D Speaker Driver
  - SNR 96dB
  - Sampling rate 8~96kHz
  - Build-in Class-D Speaker Amplifier:500mW@4Ω
- 1 x 16bit ADC
  - SNR 98dB
  - Sampling rate 8~96kHz

Bluetooth

- Dual-mode BT6.0 (DN Q334307)
- Support AoA
- Maximum transmitting power 13dBm
- Receiver sensitivity
  - -95dBm @BR
  - -95dBm @EDR Π/4 DQPSK
  - -87.5dBm @EDR 8DPSK

Graphics

- Built-in 2.5D GPU
- Multiple layer blending
- Bilinear filtering
- Smooth scaling and rotation
- 2.5D perspective transformation
- Support ARGB, RGB, AL, A, L format
- Support compressed texture format
- Support JPEG decode

Display

- Support 3/4wire SPI interface
- Support DSPI/QSPI interface
- Support 8bit MCU8080 interface

Peripherals

- 1 x Full speed USB
- 1 x SD host controller
- 4 x Multi-function 32bit timer
- 3 x UART interface
- 1 x I^2C Master/Slave interface
- 3 x SPI Master/Slave interface
- 4 x MCPWM
- 1 x QDEC
- 1 x 12bit 1MSPS ADC (16 Channel)
- 35 x GPIO Support function remapping

Sensor Hub

- 32bit CPU 24MHz
- On-chip SRAM 32kbyte
- 2 x Multi-function 32bit timer
- 2 x UART interface
- 1 x I^2C Master/Slave interface
- 1 x SPI Master/Slave interface
- 7 x LP_Touch with low power wake up

PMU

- Integrated battery charger up to 300mA
- VPWR range 4.5V to 5.5V
- VBAT range 2.7V to 4.5V
- IOVDD range 2.7V to 3.6V
- 1 x LCD power gate
- 1 x Motor power gate
- Support temperature sensor

Packages

- QFN52(6mm*6mm)

Temperature

- Operating temperature
  TC = -20℃ to +85℃(standard range)
  TC = -40℃ to +105℃(extended range)
- Storage temperature -65℃ to +150℃

Applications

- Bluetooth Watch
- Smart wear
- Color screen charging case
- Color screen e-cigarette

1 Block Diagram

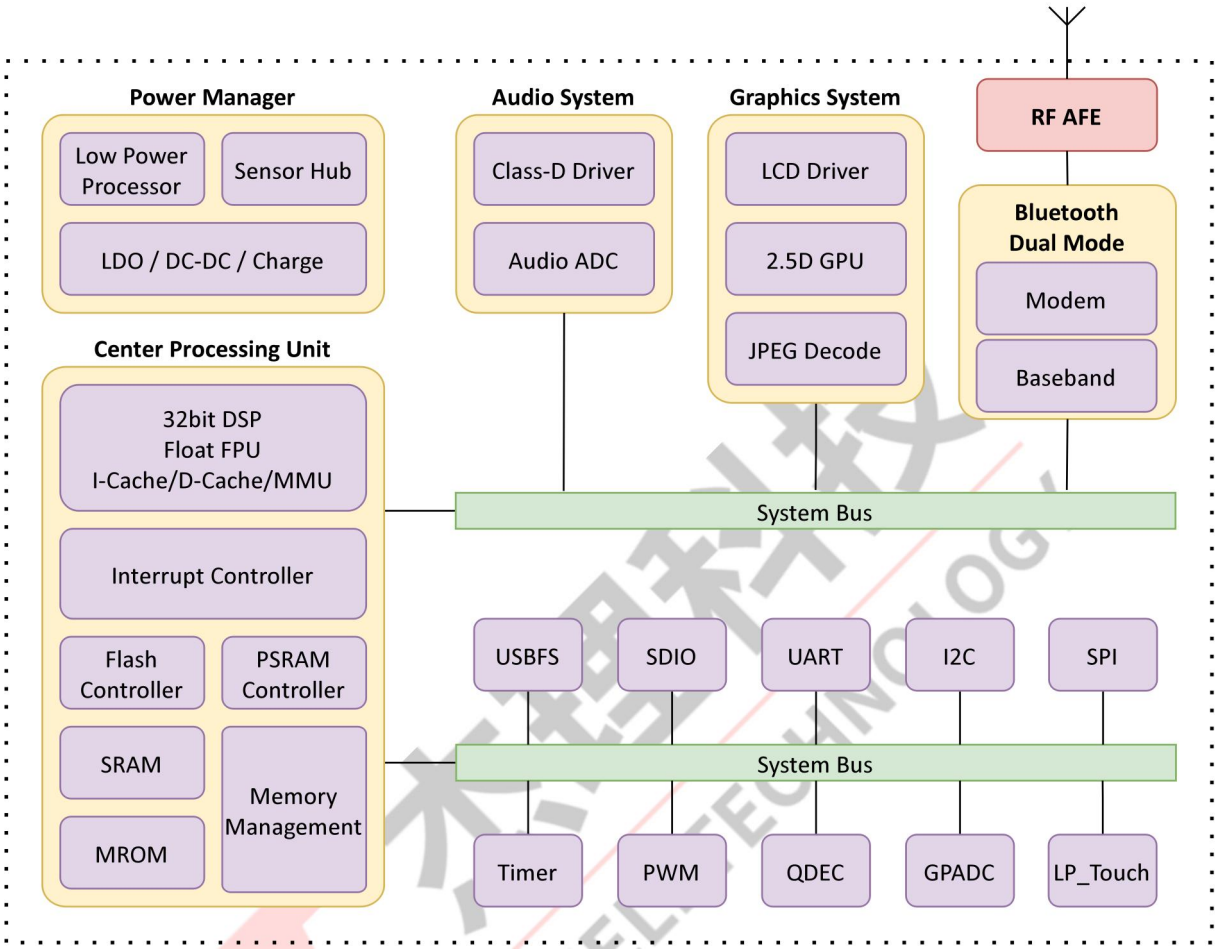


Figure 1-1 AC7072A Block Diagram

2 Pin Definition

2.1 Pin Assignment

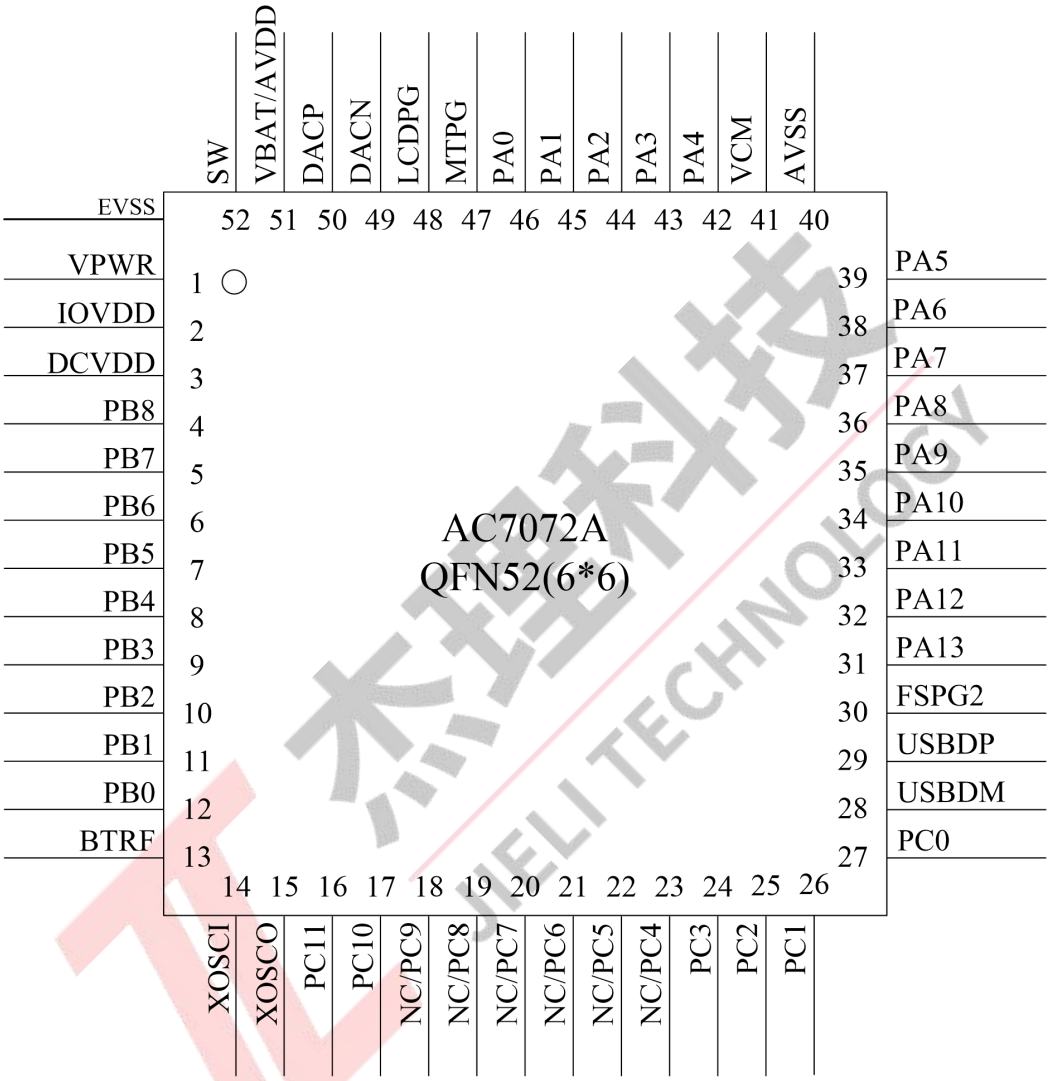


Figure 2-1 AC7072A Pin Assignment

2.2 Pin Description

Table 2-2-1 AC7072A Pin Description

Pin No.	Name	Type	IO Initial State	Description
1	VPWR	P	--	Charge Power Input
2	IOVDD	P	--	IO Power
3	DCVDD	P	--	1.25V DCDC Power
4	PB8	I/O	Z	HVTIO
5	PB7	I/O	10kΩ Pull-up	ADCP0(GPADC Input Channel P0) Hold down 0 to reset The Power key can wake up the IOVDD shutdown mode
6	PB6	I/O	Z/10kΩ Pull-up	MCLR(Device Reset,Default disable.) LP_TOUCH6(TOUCH_CH6)
7	PB5	I/O	Z	LP_TOUCH5(TOUCH_CH5)
8	PB4	I/O	Z	LP_TOUCH4(TOUCH_CH4) LVD(External Low Voltage Detection Input)
9	PB3	I/O	Z	LP_TOUCH3(TOUCH_CH3)
10	PB2	I/O	Z	LP_TOUCH2(TOUCH_CH2)
11	PB1	I/O	Z	LP_TOUCH1(TOUCH_CH1) ADC8(GPADC Input Channel 8)
12	PB0	I/O	Z	LP_TOUCH0(TOUCH_CH0) ADC7(GPADC Input Channel 7) Signal pin support external NTC (100kΩ@25℃)
13	BTRF	RF	--	Bluetooth RF Antenna
14	XOSCI	I	--	Crystal Oscillator Input
15	XOSCO	O	--	Crystal Oscillator Output
16	PC11	I/O	Z	ADC12(GPADC Input Channel 12)
17	PC10	I/O	Z	ADC11(GPADC Input Channel 11) DBI RDX
18	PC9 NC	I/O	Z	ESPI DATA0	For the model with integrated PSRAM, this pin is not connected.
19	PC8 NC	I/O	Z	ESPI DATA2	
20	PC7 NC	I/O	Z	ESPI DATA1	
21	PC6 NC	I/O	Z	ESPI CS	
22	PC5 NC	I/O	Z	ESPI CLK	
23	PC4 NC	I/O	Z	ESPI DATA3	
24	PC3	I/O	Z	ADC10(GPADC Input Channel 10) DBI DATA7
25	PC2	I/O	Z	ADC9(GPADC Input Channel 9) DBI DATA6
26	PC1	I/O	Z	ADC AP(GPADC Analog Positive Input Channel) DBI DATA5

Pin No.	Name	Type	IO Initial State	Description
27	PC0	I/O	Z	ADC AN(GPADC Analog Negative Input Channel) DBI DATA4
28	USBDM	I/O	15kΩ Pull-down	USB Negative Data ADC14(GPADC Input Channel 14)
29	USBDP	I/O	15kΩ Pull-down	USB Positive Data ADC13(GPADC Input Channel 13)
30	FSPG2	O	Z	External NOR FLASH Power Gate Built in PSRAM Power Gate
31	PA13	I/O	Z	ADC6(GPADC Input Channel 6) DBI MCU8080 DCX
32	PA12	I/O	Z	DBI SCL DBI WRX
33	PA11	I/O	Z	ADC5(GPADC Input Channel 5) DBI DATA3
34	PA10	I/O	Z	ADC4(GPADC Input Channel 4) DBI DATA2
35	PA9	I/O	Z	DBI DATA1 DBI 4W SPI DCX
36	PA8	I/O	Z	DBI DATA0
37	PA7	I/O	Z	DBI CSX
38	PA6	I/O	Z	Class-D Pre-driver Negative Output ADC3(GPADC Input Channel 3)
39	PA5	I/O	Z	Class-D Pre-driver Positive Output ADC2(GPADC Input Channel 2)
40	AVSS	G	--	Audio Ground
41	VCM	P	--	Audio reference voltage
42	PA4	I/O	Z	AIN_A0(Audio ADC Positive Input) MICBIAS(MIC Bias Output)
43	PA3	I/O	Z	AIN_A1(Audio ADC Positive Input)
44	PA2	I/O	Z	AIN_A2(Audio ADC Positive Input) AIN_AN(Audio ADC Negative Input)
45	PA1	I/O	Z	ADC1(GPADC Input Channel 1)
46	PA0	I/O	Z	ADC0(GPADC Input Channel 0)
47	MTPG	O	Z	Power gate of Motor
48	LCDPG	O	Z	Power gate of LCD
49	DACN	O	Z	Class-D Speaker Driver Negative Output
50	DACP	O	Z	Class-D Speaker Driver Positive Output
51	AVDD	P	--	Class-D Speaker Driver Power
	VBAT	P	--	Battery Input
52	SW	P	--	Buck DCDC Switch Port

Note

1.IO initial state abbreviations Z--High resistance, H--High level, L--Low level, X--May be changed during power on.

2.Timer, MCPWM, QDEC, UART, I²C, SPI and SDIO functions can be remapped to any I/O.

3.For the model with integrated PSRAM, the PC4 - PC9 pins are not connected.

Table 2-2-2 Pin Types Description

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
G	Ground	I	Input
RF	RF antenna	O	Output

Table 2-2-3 IO In Maskrom Flow Description

IO	Description
none	--

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-20	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	4.5	V
VPWR		-0.3	6	V
IOVDD		-0.3	3.6	V
DCVDD		-0.3	1.5	V
AVDD		-0.3	6	V
GPIO	Input voltage of GPIO (except PB8, LCDPG, MTPG)	-0.3	3.6	V
HVTIO	Input voltage of HVT-IO (PB8, LCDPG, MTPG)	-0.3	6	V

Note

1.Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

3.2 ESD Ratings

Table 3-2 ESD Ratings

Parameter	Typ	Test pin	Reference standard
Human Body Mode	±4kV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±300V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2kV	All pins	ANSI/ESDA/JEDEC JS-002-2022

3.3 PMU Characteristics

Table 3-3 PMU Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Power supply	--	2.7	3.7	4.5	V
VPWR	Power supply	--	4.5	5.0	5.5	V
Operating mode						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
IOVDD	Voltage output	--	--	3	3.6	V
	Loading current	IOVDD=3.0V@VBAT = 3.7V or VPWR=5v	--	--	200	mA
DCVDD	Voltage output	--	--	1.25	--	V
	Loading current	DCVDD=1.25V@IOVDD=3.0v in LDO mode	--	--	120	mA
		DCVDD=1.25V@VBAT=3.7v in DCDC mode	--	--	120	mA
Low Power mode						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
IOVDD	Loading current	IOVDD=3.0V@VBAT = 3.7v or VPWR=5v	--	--	10	mA

3.3.1 Battery Charge

Table 3-3-1 Charger Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VPWR	Charge Input Voltage	4.5	5	5.5	V
CV	CV Mode Voltage Accuracy	4.175	4.2	4.225	V
		4.325	4.35	4.375	V
		4.475	4.50	4.525	V
CC	CC Mode Current	40	--	300	mA
I_{end}	End Of Charge Current	4	--	30	mA
V_{Trikl}	Trickle Charge Voltage	--	3	--	V

3.3.2 LCDPG and MTPG Characteristics

Table 3-3-2-1 LCD Power Gate Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Ron	Pull-down Resistance	--	2.5	--	Ω
Imax	Max current at turn on state	--	--	120	mA
Vmax_off	LCDPG is turned off. Max voltage of LCDPG.	--	--	5.5	V

Table 3-3-2-2 MT Power Gate Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Ron	Pull-down Resistance	--	2.5	--	Ω
Imax	Max current at turn on state	--	--	160	mA

Symbol	Parameter	Min	Typ	Max	Unit
Vmax_off	MTPG is turned off. Max voltage of MTPG.	--	--	5.5	V

3.3.3 FSPG2 Characteristics

Table 3-3-3 NOR FLASH/PSRAM Power Gate Characteristics

Symbol	Parameter	Conditions	Typ	Unit
R_{pd}	Pull-down Resistance	IOVDD = 3.0V	10k(PD=1) 100k(PD=2) 1M(PD=3)	Ω
Imax	Max current at turn on state	IOVDD = 3.0V	30	mA

3.4 IO Characteristics

Table 3-4 IO Characteristics

Input Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Min**	**Max**	**Unit**
V_{IL}	Low-Level Input Voltage	IOVDD = 3.0V	PA0~PA13 PB0~PB8 PC0~PC11 USBDP USBDM VPWR	-0.3	1.3	V
V_{IH}	High-Level Input Voltage	IOVDD = 3.0V	PA0~PA13 PB0~PB7 PC0~PC11 USBDP USBDM	1.7	3.3	V
		IOVDD = 3.0V	PB8 VPWR	1.7	5.5	V
Output Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Typ**		**Unit**
| I_{OL} |	Output Current	IOVDD = 3.0V Voutput = 0.3V	PA0~PA13 PB0~PB7 PC0~PC11	4(HD=0) 8(HD=1) 16(HD=2) 32(HD=3)		mA
		IOVDD = 3.0V Voutput = 0.3V	PB8 USBDP USBDM	8		mA
		IOVDD = 3.0V Voutput = 0.3V	VPWR	2		mA
| I_{OH} |	Output Current	IOVDD = 3.0V Voutput = 2.7V	PA0~PA13 PB0~PB7 PC0~PC11	4(HD=0) 8(HD=1) 16(HD=2) 32(HD=3)		mA
		IOVDD = 3.0V Voutput = 2.7V	PB8 USBDP USBDM	8		mA
		IOVDD = 3.0V Voutput = 2.7V	VPWR	2		mA
Internal Resistance Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Typ**		**Unit**
R_{pu}	Pull-up Resistance	IOVDD = 3.0V	PA0~PA13 PB0~PB8 PC0~PC11	10k(PU=1) 100k(PU=2) 1M(PU=3)		Ω

			VPWR		
		IOVDD = 3.0V	USBDP	1.5k	Ω
		IOVDD = 3.0V	USBDM	180k	Ω
R_{pd}	Pull-down Resistance	IOVDD = 3.0V	PA0~PA13 PB0~PB8 PC0~PC11 VPWR	10k(PD=1) 100k(PD=2) 1M(PD=3)	Ω
		IOVDD = 3.0V	USBDP USBDM	15k	Ω

Note

1. Internal pull-up/pull-down resistance accuracy ±20%

3.5 Class-D Speaker Driver Characteristics

Table 3-5 Class-D Speaker Driver Characteristics Under AVDD 3.7v

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bit
Output Sample Rate	--	8	--	96	kHz
SNR	Pre-drive differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	98	--	dB
	Pre-drive Single-ended Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	90	--	dB
	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=8Ω	--	96	--	dB
THD+N	Pre-drive differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	-72	--	dB
	Pre-drive single-ended Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	-48	--	dB
	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=8Ω	--	-45	--	dB
Noise Floor	Pre-drive differential Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	13	--	uVrms

Parameter	Conditions	Min	Typ	Max	Unit
	Pre-drive single-ended Mode Fin=1kHz@0dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	19	--	uVrms
	Differential Mode B/W=20Hz~20kHz A-Weighted load=8Ω	--	26	--	uVrms
Dynamic Range	Pre-drive differential Mode Fin=1kHz@-60dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	95	--	dB
	Pre-drive single-ended Mode Fin=1kHz@-60dBFS Fs=48kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	90	--	dB
	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=8Ω	--	90	--	dB
Max Output Power	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=4Ω	--	500	--	mW

3.6 Audio ADC Characteristics

Table 3-6 Audio ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	16	--	bit
Output Sample Rate	--	8	--	96	kHz
SNR	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	98	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	97	--	dB
Dynamic Range	Differential input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	98	--	dB
	Single-ended input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	97	--	dB
THD+N	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-83	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=0dB	--	-80	--	dB
Analogue Gain	--	-6		27	dB
Max Input Level	Differential input Mode ADC gain=0dB	--	2	--	Vrms
	Single-ended input Mode ADC gain=0dB	--	1	--	Vrms

3.7 BT Characteristics

3.7.1 Transmitter

Table 3-7-1-1 Transmitter characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Maximum RF Transmit Power	BR	--	10	13	dBm
Maximum RF Transmit Power	EDR Π/4 DQPSK EDR 8DPSK	--	10	--	dBm
Relative Transmit Power	EDR Π/4 DQPSK EDR 8DPSK	--	-3	--	dB
Maximum RF Transmit Power	BLE-1Mbps	--	10	13	dBm

3.7.2 Receiver

Table 3-7-2 Receiver characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity	BR	--	-95	--	dBm
	EDR Π/4 DQPSK	--	-95	--	dBm
	EDR 8DPSK	--	-87.5	--	dBm
	BLE-1Mbps	--	-98	--	dBm
	BLE-2Mbps	--	-95	--	dBm

3.8 12bit GPADC Characteristics

Table 3-8-1 12bit GPADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
AVDD(ADC Supply Voltage)	AVDD=IOVDD	1.8	3	3.6	V
I_{AVDD}(Current of the ADC on AVDD)	Single-ended f_{ADC} =12MHz AVDD=AVREF=3V	--	310	--	uA
	Diff-ended with DiffAMP f_{ADC} =12MHz AVDD=AVREF=3V	--	780	--	uA
f_{ADC}(ADC Clock Frequency)	--	0.25	--	12	MHz
Ts(ADC Sampling Time)	--	1.5	--	--	$1/f_{ADC}$
ADC Conversion Time	Including Sampling Time	8	14	14	$1/f_{ADC}$
ADC Input Voltage Range	--	0	--	AVREF	V
ADC Internal Sample and Hold Capacitor	--	--	--	5	pF
Sampling Switch Resistance	--	--	--	1	kΩ
External Input Impedance	Ts=1.5/f_{ADC}	--	--	1.5	kΩ
	Ts>=50/f_{ADC}	--	--	50	kΩ
ADC Resolution	Programmable	6	12	12	bit
INL	AVDD=3V, f_{ADC}=12MHz	-1	--	3	LSB

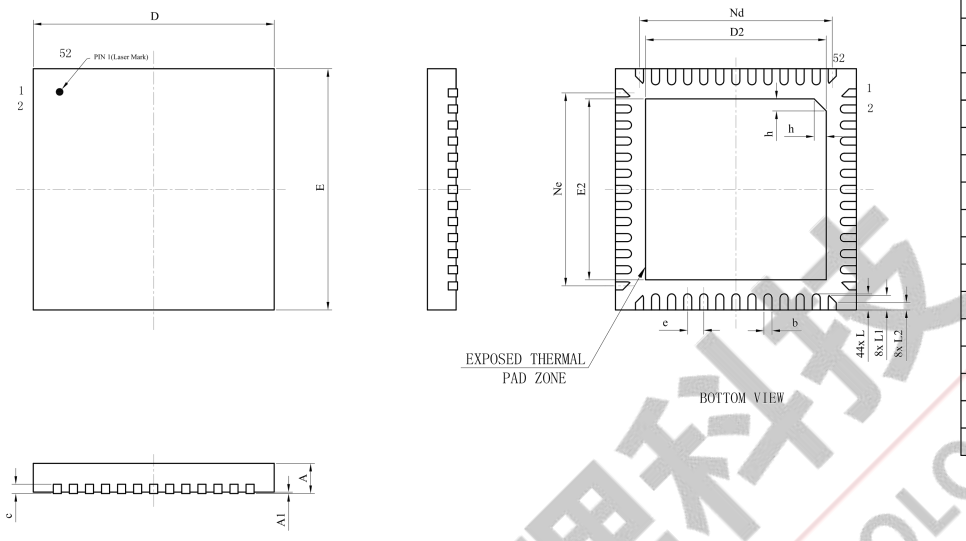
DNL	AVDD=3V, f_{ADC}=12MHz	-1	--	1	LSB
ADC Offset Error	AVDD=3V, f_{ADC}=12MHz	--	--	2.4	LSB
Gain Error	AVDD=3V, f_{ADC}=12MHz	--	--	5.8	LSB
ENOB(Effective number of bits)	Single-ended AVDD=AVREF=3V fIN =1kHz, f_{ADC}=12MHz	--	10.6	--	bit
	Diff-ended with DiffAMP AVDD=AVREF=3V fIN =1kHz, f_{ADC}=12MHz	--	11	--	bit

Table 3-8-2 12bit ADC Characteristics

Tsample(1/f_{ADC})	Tsample(us)	Max.Rext-input(kΩ)
1.5	0.125	1.5
2.5	0.209	3.3
3.5	0.291	5.0
4.5	0.375	6.7
6.5	0.542	10.1
8.5	0.708	13.6
12.5	1.042	20.4
16.5	1.375	27.3
24.5	2.042	41.0
32.5	2.708	54.8
48.5	4.042	82.3
64.5	5.375	109.7
128.5	10.708	219.7
256.5	21.375	439.5
1024.5	85.375	1758.5
4096.5	341.375	7034.7

4 Package Information

4.1 QFN52_6×6mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 4-1 AC7072A Package

5 IC Marking Information

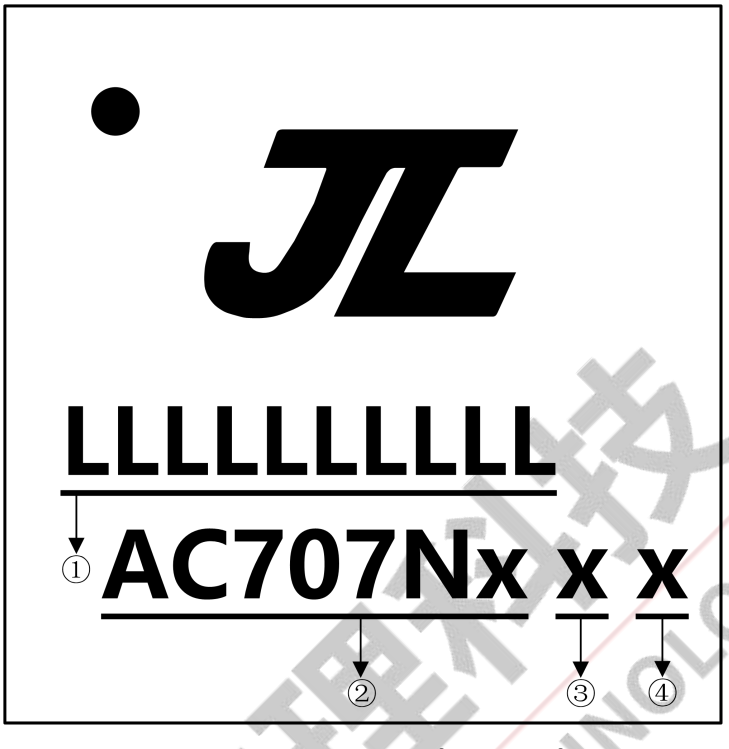


Figure 5-1 AC7072A Package Outline

① LLLLLLLLL: Production Batch
② AC707Nx: Chip Model
③ x: Built-in flash size
0: No Flash Memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash
5: 64Mbit Flash
7: 128Mbit Flash
④ x: Built-in PSRAM size
Space: No PSRAM Memory
S: 16Mbit PSRAM
T: 64Mbit PSRAM

6 Solder-Reflow Condition

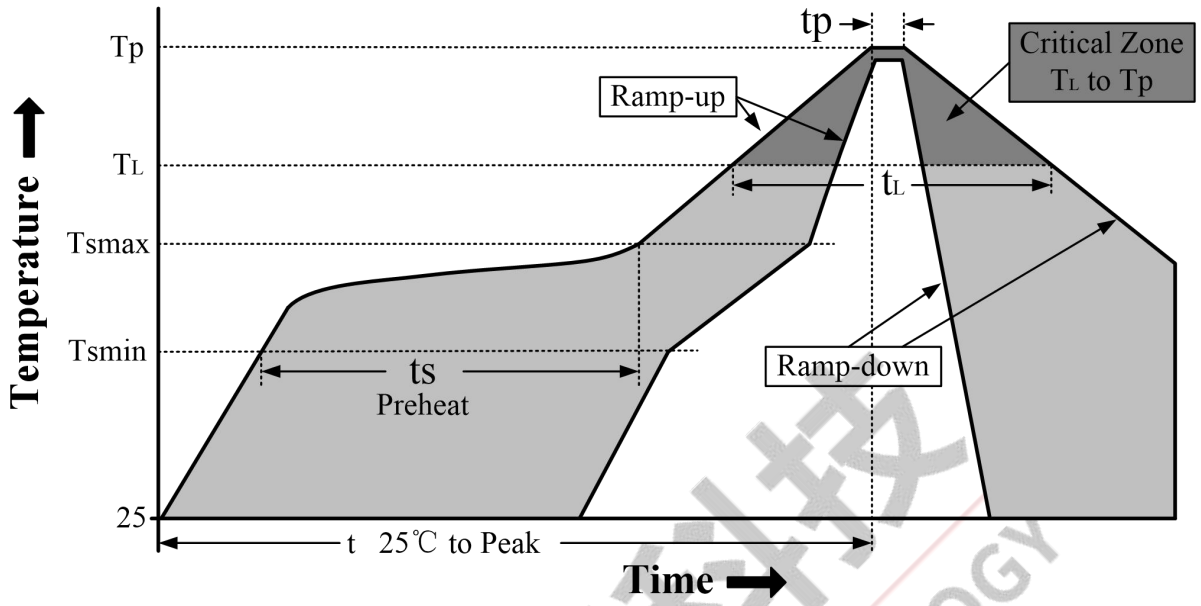


Figure 6-1 Classification Reflow Profile

Table 6-1 Classification Profiles

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min (T_{smin})	100℃	150℃
	Temperature Max (T_{smax})	150℃	200℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5℃ of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6℃/second max	6℃/second max
Time 25℃ to peak temperature		6 minutes max	8 minutes max

Note

1.All temperatures refer to topside of the package, measured on the package body surface

2.Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" and "user" maximum.

Table 6-2 SnPb Classification Temperature

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
≥2.5 mm	225 +0/-5℃	225 +0/-5℃

Table 6-3 Pb-free - Classification Temperature

Package Thickness	Volume mm³ < 350	Volume mm³ 350 - 2000	Volume mm³ > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

Note

1.*Tolerance The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0℃.For example 260℃+0℃)at the rated MSL level.

7 Storage Condition

7.1 Moisture Sensitivity Level

AC707N is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at＜40°C and 90% relative humidity (RH).
2. Peak package body temperature≤260°C.
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions≤30°C/60%RH or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads＞10% for level 2a-5a devices or＞60% for level 2 devices when read at 23±5°C,or 3a or 3b are not met.
5. Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.