AC1299A Datasheet

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Version：1.1

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AC1299A Features

CPU

- 32bit DSP
- Maximum speed 192MHz
- 8 Levels interrupt priority

Memory

- ROM
- Optional built-in flash memory

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock

DSP Audio Processing

- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC
  SNR ≥ 98dB@730mVrms
- One channel 16-bit ADC
  SNR ≥ 95dB@1Vrms
- Audio DAC Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/ 32KHz/44.1KHz/48KHz/64KHz/88.2KHz/ 96KHz are supported
- Audio ADC Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/ 32KHz/44.1KHz/48KHz are supported
- Audio DAC support single-ended and differential cap-less mode
- Support AMUX and ADC to DAC
- Support for driving 16 or 32 ohm Speaker

Peripherals

- One full speed USB OTG controller
- One SD host controller for MMC/SD
- Three multi-function 32-bit timers, support capture and PWM mode
- UART controller supports DMA
- One IIC Master controller
- Two SPI Master / Slaver controller with DMA
- One QDEC interface
- 7-channel 10-bit general purpose ADC
- Two pairs MCPWM
- 7 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Up to 7 external interrupt / wake-up source (low power available,can be multiplexed to any I/O)

PMU

- VPWR range : 2.7V to 5.5V
- IOVDD range : 2.1V to 3.6V

Packages

- QFN16(3mm*3mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- USB Headset

1 Block Diagram

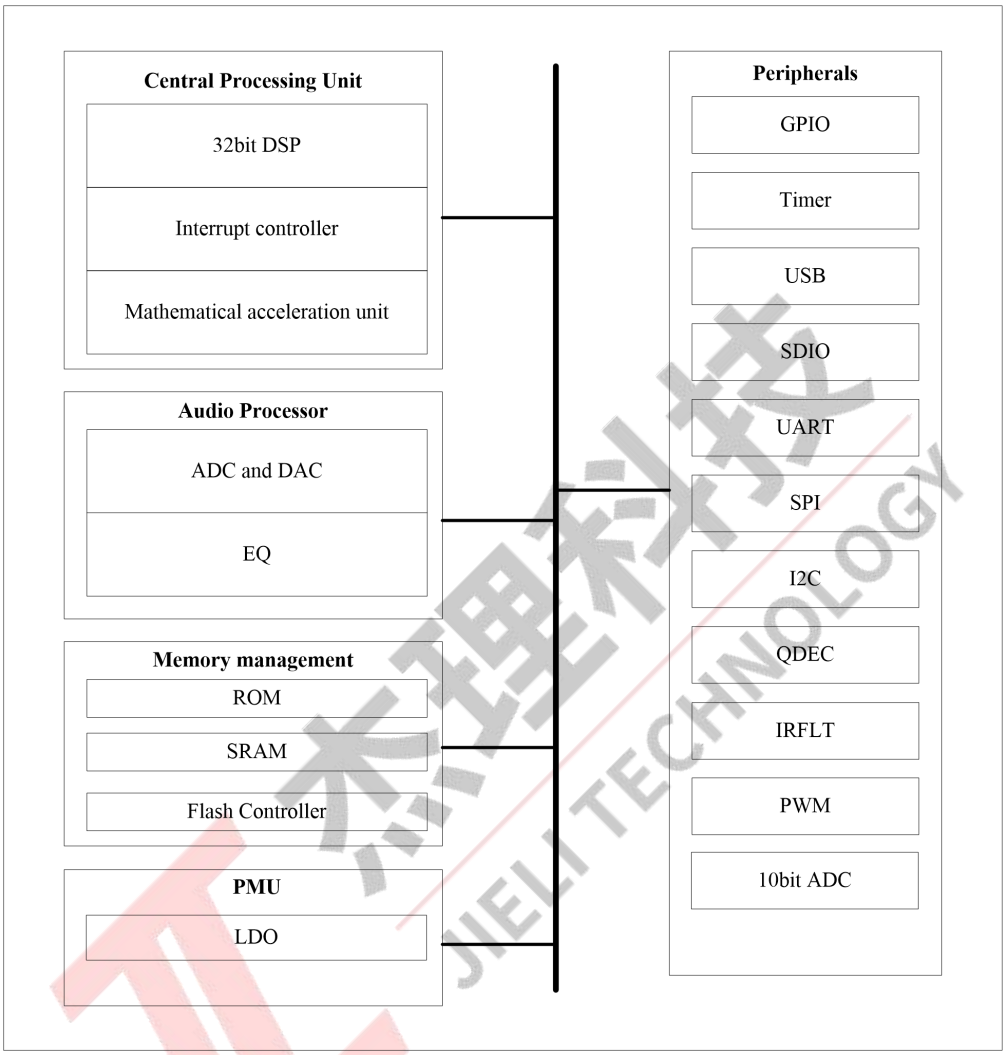


Figure 1-1 AC1299A Block Diagram

2 Pin Definition

2.1 Pin Assignment

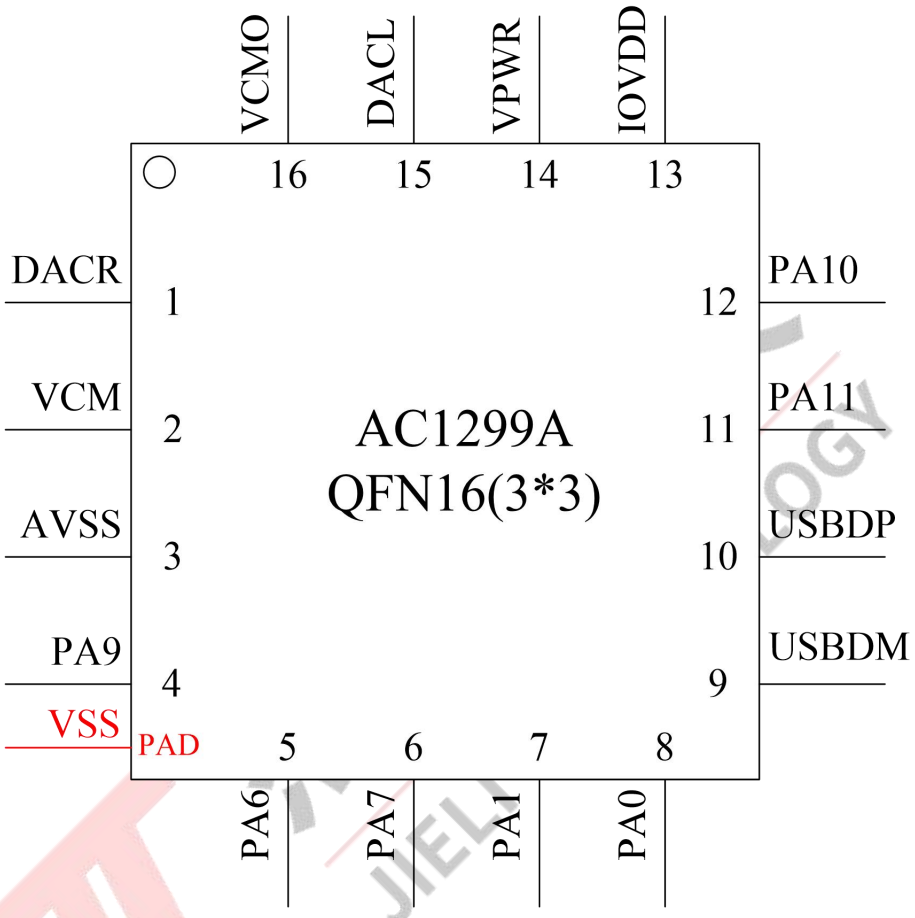


Figure 2-1 AC1299A Package Diagram

2.2 Pin Description

Table 2-1 AC1299A Pin Description

PIN NO.	Name	Type	Function	Other Function
1	DACR	AO		Right channel audio output;
2	VCM	P		Audio analog reference bias;
3	AVSS	G		Audio ground;
4	PA9	I/O	GPIO	ADC9:ADC Input Channel 9; MICLDO:MIC linear voltage regulator output; MIC_BIAS:MIC Bias Output(Built-in resistor);
5	PA6	I/O	GPIO	ADC6:ADC Input Channel 6; AIN_N:Different MIC Negative; AUX2:Analog input Channel 2；
6	PA7	I/O	GPIO	ADC7:ADC Input Channel 7; MICIN:MIC Input Channe; AUX1:Analog input Channel 1；
7	PA1	I/O	GPIO (pull up)	Long press reset; MCLR; ADC1:ADC Input Channel 1;
8	PA0	I/O	GPIO	ADC0:ADC Input Channel 0;
9	UDBDM	I/O	USB Negative Data (pull down)	ADC15:ADC Input Channel 15;
10	USBDP	I/O	USB Positive Data (pull down)	ADC14:ADC Input Channel 14;
11	PA11	I/O	GPIO	ADC11:ADC Input Channel 11;
12	PA10	I/O	GPIO	ADC10:ADC Input Channel 10; LVD:Low Voltage Detect;
13	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
14	VPWR	PI		Power supply input;
15	DACL	AO		Left channel audio output;
16	VCMO	AO		Reference output of the audio;
PAD	VSS	G		System ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	I	Input
PO	Power Output	O	Output
AO	Analog Output	G	Ground

CROSSBAR						
SPI1	**SDC**	**IIC**	**Q-decoder**	**UART0**	**UART1**	**MCPWM**
SPI1_CLK	SD_CLK	IIC_CLK	Q-decoder 0	UART0_TX	UART1_TX	PWMCH0H
SPI1_DI	SD_CMD	IIC_DAT	Q-decoder 1	UART0_RX	UART1_RX	PWMCH0L
SPI1_D0	SD_DAT				UART1_CTS	PWMCH1H
SPI1_DAT2					UART1_RTS	PWMCH1L
SPI1_DAT3						M_TMR0CK
						M_TMR1CK

Input Channel x8			Output Channel x8	
Timer0	CAP0	IRFLT	PWM0	CLK_OUT0
Timer1	CAP1		PWM1	CLK_OUT1
Timer2	CAP2		PWM2	CLK_OUT2
				CLK_OUT3

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VPWR	Power supply input	-0.3	6.0	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 ESD Protectio

Table 3-2

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

3.3 PMU Characteristics

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charger supply Voltage	2.7	5.0	5.5	V	_
IOVDD	Voltage output	2.1	3.0	3.6	V	VPWR = 4.2V, 10mA loading
	Loading current	_	_	100	mA	IOVDD=3.3V@VPWR = 3.6V
V_{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
GPIO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Input Voltage	_	_	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Input Voltage	0.9*IOVDD	_	_	V	IOVDD= 3.0V

3.5 IO Output Drive Strength Pull Up/Down Characteristics

Table 3-5

Port	**Drive Strength**	**Pull Up Resistance**	**Pull DownResistance**	**Test Conditions**
PA0,PA1 PA6,PA7 PA9,PA10,PA11	00: 3mA 01: 9mA 10: 21mA 11: 50mA	10K/100K/1M	10K/100K/1M	IOVDD = 3.3V
DP	8mA	1.5K	15K	IOVDD = 3.3V
DM	8mA	180K	15K	IOVDD = 3.3V

Note1: precision of 10K/100K pull-up and pull-down resistor is ±30%

Note2: precision of 1M pull-up and pull-down resistor is ±50%

Note3: PA1 default pull up,USBDM and USBDP default pull down

3.6 Audio DAC Characteristics

Table 3-6

Parameter	Loading	Min	Typ	Max	Unit	Test Conditions
Frequency Response		20	_	20K	Hz	VPWR=5.0V Fin=1KHz/0dB B/W=20Hz~20kHz A-Weighted Filter
Output Swing	10kohm	_	740	_	mVrms	
	32ohm	_	730	_	mVrms	
	16ohm	_	640	_	mVrms	
THD+N	10kohm	_	-77	_	dB	
	32ohm	_	-65	_	dB	
	16ohm	_	-65	_	dB	
S/N	10kohm	_	98	_	dB	
	32ohm	_	98	_	dB	
	16ohm	_	97	_	dB	
Dynamic Range	10kohm	_	92	_	dB	VPWR=5.0V Fin=1KHz/-60dB B/W=20Hz~20kHz A-Weighted Filter
	32ohm	_	92	_	dB	
	16ohm	_	91	_	dB	
Noise Floor	10kohm	_	10	_	uVrms	VPWR=5.0V B/W=20Hz~20kHz A-Weighted Filter
	32ohm	_	10	_	uVrms	
	16ohm	_	10	_	uVrms	
Noise Floor with MUTE	10kohm	_	6	_	uVrms	VPWR=5.0V B/W=20Hz~20kHz A-Weighted Filter
	32ohm	_	6	_	uVrms	
	16ohm	_	6	_	uVrms	
Crosstalk	10kohm	_	-110	_	dB	VPWR=5.0V Fin=1KHz/0dB
	32ohm	_	-64	_	dB	
	16ohm	_	-60	_	dB	
Output Power	32ohm	_	16.5	_	mW	Fin=1KHz THD+N < 0.1%
	16ohm	_	25.5	_	mW	

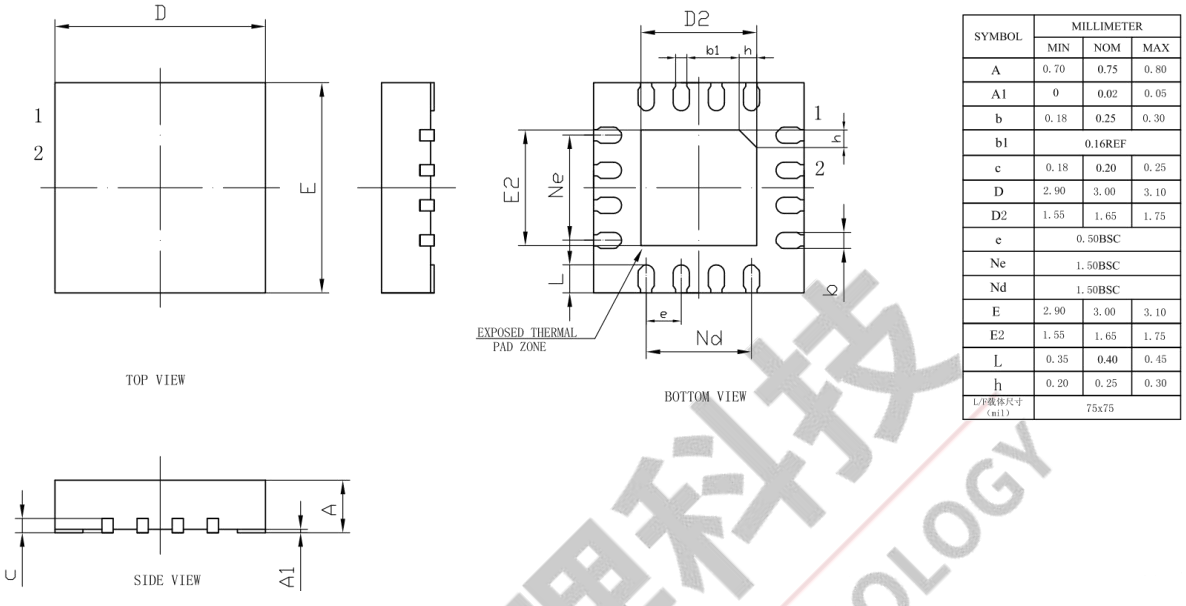
3.7 Audio ADC Characteristics

Table 3-7

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	Differential	_	79@VCM cap	_	dB	Gain=28dB,Fsample=44.1KHz Fin=1KHz @64mVrms A-wt B/W=20Hz-20KHz
		_	75@VCM capless	_	dB	
	Single-ended	_	77@VCM cap	_	dB	Gain=23dB,Fsample=44.1KHz Fin=1KHz @57mVrms A-wt B/W=20Hz-20KHz
		_	72@VCM capless	_	dB	
S/N	Differential	_	78@VCM cap	_	dB	Gain=28dB,Fsample=44.1KHz Fin=1KHz @64mVrms A-wt B/W=20Hz-20KHz
		_	73@VCM capless	_	dB	
	Single-ended	_	76@VCM cap	_	dB	Gain=23dB,Fsample=44.1KHz Fin=1KHz @57mVrms A-wt B/W=20Hz-20KHz
		_	71@VCM capless	_	dB	
THD+N	Differential	_	-69@VCM cap	_	dB	Gain=28dB,Fsample=44.1KHz Fin=1KHz @64mVrms A-wt B/W=20Hz-20KHz
		_	-67@VCM capless	_	dB	
	Single-ended	_	-73@VCM cap	_	dB	Gain=23dB,Fsample=44.1KHz Fin=1KHz @57mVrms A-wt B/W=20Hz-20KHz
		_	-68@VCM capless	_	dB	

4 Package Information

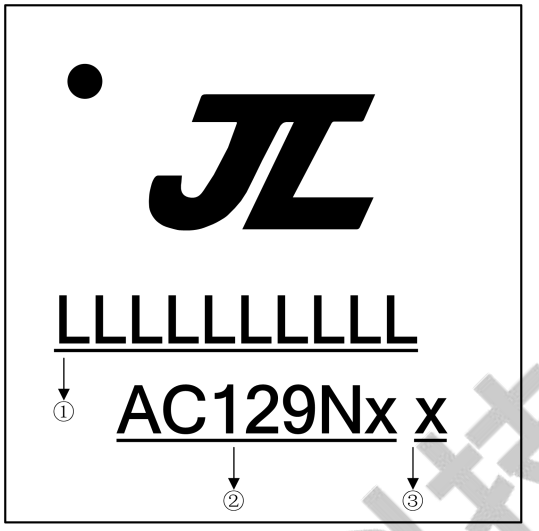
4.1 QFN16_3×3mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸（mil）	75x75		

Figure 4-1 AC1299A Package

5 IC Marking Information



① LLLLLLLLLL：Production Batch
② AC129Nx：Chip Model
③ Built-in flash size
0: No Flash Memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash

6 Solder-Reflow Condition

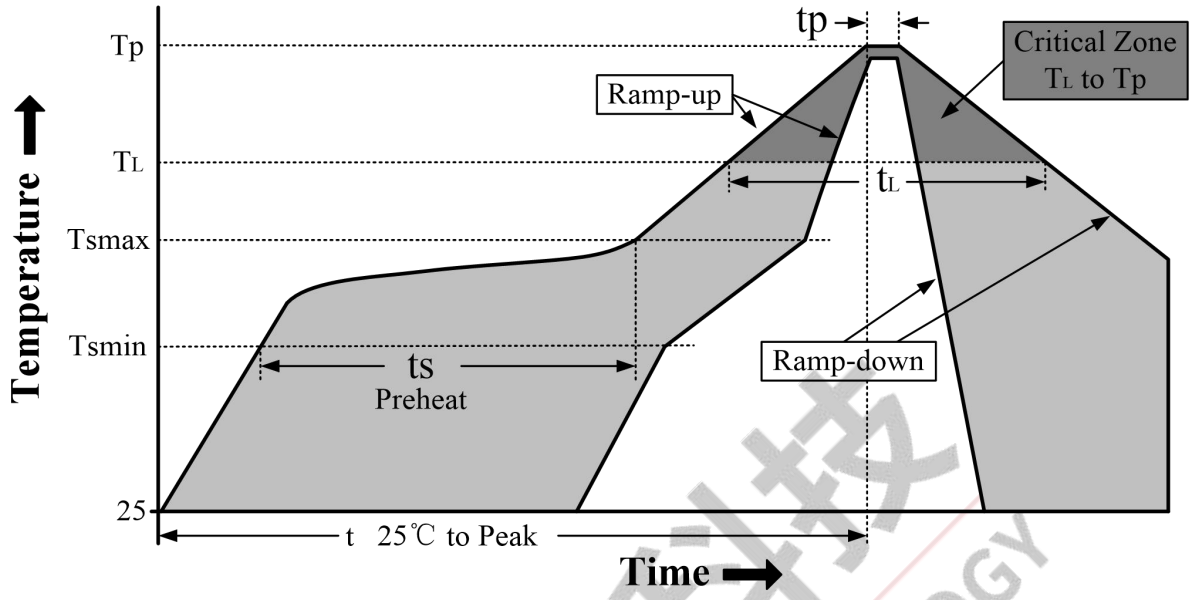


Figure 6-1 Classification Reflow Profile

Classification Profiles **Table 6-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 ℃	150 ℃
	Temperature Max (T_{smax})	150 ℃	200 ℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 ℃/second max	3 ℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183 ℃ 60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (tp)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 ℃/second max.	6 ℃/second max.
Time 25 ℃ to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature **Table 6-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 ℃	225 +0/-5 ℃
≥ 2.5 mm	225 +0/-5 ℃	225 +0/-5 ℃

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5mm	260 ℃	250 ℃	245 ℃
> 2.5mm	250 ℃	245 ℃	245 ℃

7 Storage Condition

7.1 Moisture Sensitivity Level

AC1299A is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at＜40°C and 90% relative humidity (RH).
2. Peak package body temperature≤260°C.
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions≤30°C/60%RH or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads ＞ 10% for level 2a-5a devices or＞60% for level 2 devices when read at 23±5°C,or 3a or 3b are not met.

Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.

8 Revision History

Date	Revision	Description
2023.11.27	V1.0	Initial Release.
2025.11.24	V1.1	Add DAC Noise Floor with MUTE Parameter.